ENGINEERING SURFACE MORPHOLOGY AT THE ATOMIC LEVEL WITH APPLICATIONS IN ELECTRONIC MATERIALS

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The silicon (111) and (001) surfaces have wide technological importance. Control of the morphologies of these surfaces at the atomic level is vital for such applications as layer-by-layer growth or assembly of nano-scale devices. We have developed techniques to create large areas with no or widely spaced atomic steps on patterned silicon surfaces by high temperature annealing in ultra-high vacuum (UHV).

At annealing temperatures high enough to promote surface premelting, large liquid-like structures form and are preserved during quenching on regions with low step-density since these areas have no efficient sinks to absorb diffusing atoms. Based on the surface morphologies observed by atomic force microscopy, we suggest a sequence of events for the evolution of the silicon surface, from the onset of surface premelting up to the bulk melting temperature. Large dendritic islands observed on the more slowly cooled down Si(111) samples are attributed to the persistence of surface melted structures and to non-equilibrium 'condensation' of the excess adatoms from the (1x1) → (7x7) phase transition.

The effect of UHV high temperature annealing on the Si(111) surface is an initial increase in the measured surface roughness due to Ostwald ripening followed by a surface smoothing to become atomically flat. The boundaries of etched craters or mesas initially develop profiles upon annealing that conform to the predictions of continuum theory of surface transport.

As an application, we built MOS capacitors on three types of Si(111) surfaces viz. atomically flat surfaces, normal (stepped) surfaces cleaned in UHV by high-temperature annealing and normal, RCA cleaned wafer surfaces. The leakage current through the oxide was measured for all three cases. Our results show that the smoother the surface before oxidation, the smaller the leakage current.

In another application Si(111) substrates with regular arrays of atomic steps were used to induce azimuthal alignment of crystals in thin pentacene films. Pentacene films deposited on heated samples, at a low deposition rate, show significant azimuthal alignment of the pentacene crystals relative to the atomic steps, with the (110) pentacene planes being parallel to the atomic steps.

BIOGRAPHICAL SKETCH

Valerian Ignatescu was born in Suceava, a city in northern Romania. His high school education was received at “Stefan cel Mare” National College (founded in 1860). After a six months required military service (1989-1990) he started a long “career” as a student during which he first acquired a Bachelor of Science in Mechanical Engineering in 1995 from “Gh. Asachi” University of Iasi (Romania). He was admitted in 1994 to the “Al. I. Cuza” University of Iasi (Romania) where he obtained another Bachelor of Science degree in Applied Physics (1999), a Master of Science in Plasma Physics (1999), and he even started a doctorate in Physics, which he completed in 2004, during his only visit to Romania since August 2002 when he arrived at Cornell University for a Doctor of Philosophy degree in Materials Science and Engineering.

He received a Master of Science in Materials Science and Engineering in January 2005 and he expects to be conferred the Doctor of Philosophy degree in this field in August 2007. Starting July 2007 he will begin working as process engineer at Intel.

To my whole family

and especially to my dear departed sister.

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I am especially grateful to my advisor, Prof. Jack M. Blakely, who provided invaluable input during these years. He not only offered me financial and moral support, but also continuous guidance, which I greatly appreciated especially in the moments when nothing seemed to make sense. He allowed me a great deal of intellectual freedom and his door was always open for any kind of issues I have had. With his calm, patience, utmost moral and scholar qualities, he will always remain an example for me to follow.

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I am grateful to my wife, Liliana Ignatescu for her relentless support and encouragement and for being with me in tranquil and tumultuous moments equally. She also gave me a wonderful son, who shines a warm light into our lives since he arrived into this world. Last but not least I would like to thank my parents and my departed grandparents who loved and fostered me. Under their guidance I developed my intellectual curiosity and I have learned the values of honesty, perseverance, hard and unabated work.

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CHAPTER 1

INTRODUCTION

1.1 Atomic steps on vicinal surfaces

The study and the control of surface morphology at the atomic level is very important for such applications as layer-by-layer growth of epitaxial overlayers or assembly of nano-scale devices. Even perfectly cleaved surfaces, from entropic reasons contain certain local surface defects such as adatoms or vacancies. Most of the available crystalline substrates are cut from ingots along particular crystallographic orientations with a certain miscut. For such vicinal surfaces the thermodynamic equilibrium structure that has to accommodate this miscut is given by an array of atomic steps (and kinks) separated ideally by atomically flat terraces (Fig. 1.1). For example if the surface is Si(001), an one monolayer-height atomic step has 1.5 Å. For a wafer miscut of 0.5°, the average terrace width would be ~17 nm (about 115 rows of atoms). An excellent review about the atomic steps in thermal equilibrium, their properties and their connection with the surface morphology was published by Jeong and Williams [1].

The easiest way these atomic steps can be moved is to use the use high temperature annealing in ultra high vacuum (UHV). The atoms placed right at the step edge are weaker bounded and therefore would preferentially detach form the step and eventually evaporate from the surface. The UHV annealing is commonly used to obtain very clean and flat surfaces. Depending on the material and on the heating procedure various types of step distributions on the surface can be obtained. In the case of silicon, large atomically flat surfaces can be engineered at the bottom of etched craters [2-4] (Fig. 1.2). Alternatively regular arrays of single atomic step [5] or step

bunches separated by microns wide flat terraces can also be obtained [6, 7] (see also Fig. 1.2).

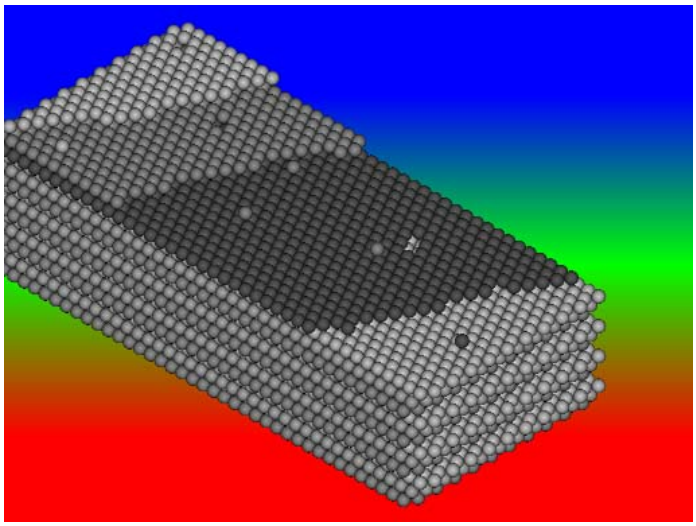

Figure 1.1. Model of an FCC vicinal surface showing steps and flat terraces.

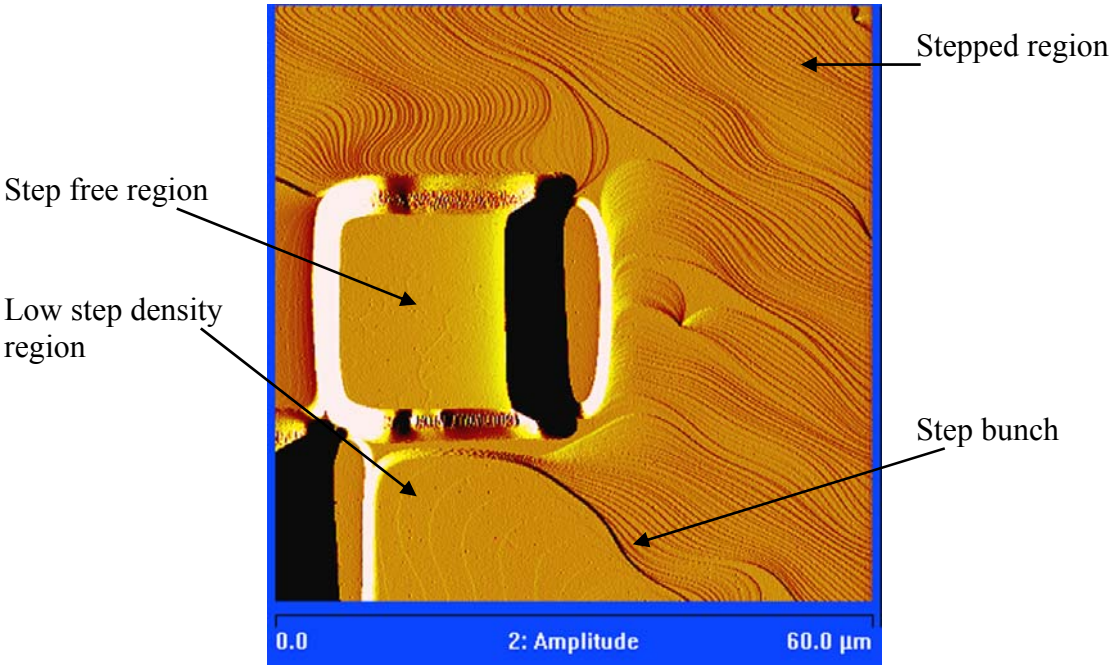

Figure 1.2. Large AFM scan showing a step-free crater surrounded by stepped regions

It should be noted that high temperature annealing in UHV is certainly not the only way to create good silicon substrates. Other alternatives include epitaxial growth [8-17], annealling in hydrogen or inert gases ambient [6, 18-24], and selective chemical etching [25-33].

In the present dissertation we will present experiments related to controlling the step distribution on silicon surfaces and two applications that we developed using our substrates processed by ultra-high vacuum (UHV) high temperature annealing.

1.2 General procedure for preparing the silicon samples

Czochralski (CZ) Si(111) wafers were RCA cleaned and then 300 nm thermal oxide was grown as a silicon etch mask using wet oxidation at 1100 °C. Utilizing standard photolithography techniques, various geometric patterns, with dimensions ranging from 10 to 120 μm, were transferred to the wafers in the form of ~ 1 μm deep craters. After the removal of the silicon oxide mask by HF, the wafers were again RCA cleaned (without performing the HF dip) in order to remove any surface contamination caused by the reactive ion etching (RIE) process. Using a scriber, 6 mm wide and 18 mm long samples were detached from the wafers. The samples were blown with nitrogen, dipped in HF, rinsed with DI water and blow dried with nitrogen. In this way a clean, hydrogen terminated surface was obtained. Each sample was loaded into the UHV chamber and heated using direct current (DC). The base pressure in the UHV chamber before starting the annealing was below 10^{-10} torr. More details about the photolithographic processing can be found in the Appendix A.1.

A typical heating procedure included a slow heating up to 900 °C so that the measured pressure inside the UHV chamber did not increase above 2×10^{-9} torr

allowing the sample and sample holder to slowly degas. One or two flashes at 1250-1300 °C were performed in order to remove all the remaining native oxide (and potentially other high melting temperature components, such as silicon carbide) from the silicon surface. The samples were then annealed at temperatures ranging from 950-1150 °C and cooled down.

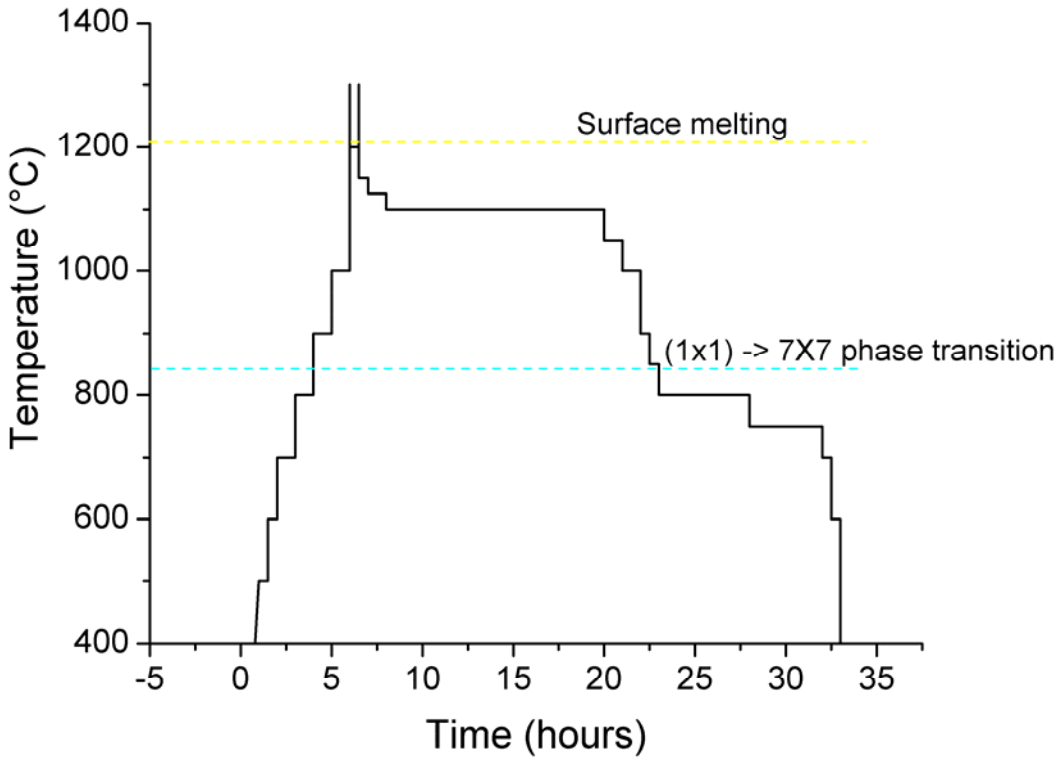

Figure 1.3. Typical annealing procedure used to obtained large step-free surfaces

Sample temperatures were measured from outside using two pyrometers, one of which was a two color (differential) pyrometer. The temperature distribution across the samples was measured by an infrared (IR) camera equipped with an InSb focal plane array detector. In order to eliminate errors due to heat radiation being absorbed

by the chamber's viewports, we recalibrated the pyrometers and the IR camera with respect to the melting temperature of silicon. Nevertheless, due to some changes in the temperature distribution across the samples (especially close to the melting point), we estimate the accuracy of the measured temperature to be ± 25 °C.

On some samples a temperature gradient was *intentionally* induced by deliberately clamping the sample tighter on the lower side so that we could investigate the influence of a continuous range of temperatures on the same sample. These samples were cut from Si(111) wafers with 0.001 Ω-cm (boron doped) and 0.1° miscut angle. By using such high conductivity silicon we could easily heat our samples by DC even if they were non-uniformly fastened. Therefore a higher temperature gradient was possible (see also Chap. 3). Although the high boron concentration (~2×10^{20} cm^{-3} in our case) is known to induce boron precipitates at the silicon surface [34-37], which in turn generate pits on the surface [38, 39], we have obtained similar surface structures to those described below on higher resistivity samples (0.8 Ω-cm).

The surface morphology was analyzed using atomic force microscopy (AFM) in open atmosphere, but in a clean-room. Even though the samples acquire a layer of native oxide, this process does not modify the surface features at the length scales revealed by AFM [40, 41]. In order to improve the step contrast some of the AFM images presented in this paper are in the amplitude (height derivative) mode. This mode generates on AFM images an apparent illumination effect. In our amplitude images the apparent shadows are such that the "light" seems to come from the right, meaning that a bright step accounts for a step up from the right to the left.

1.3 Motivation and overview of the dissertation

The behavior of silicon surfaces was intensively analyzed in all the temperature ranges up to the bulk melting point. Most of studies on the morphologies of the high temperature surface phases are based on diffraction methods, which preclude the possibility to locally analyze the structures that appear and develop on the surface during those phase transitions. The only methods that can directly and locally probe in-situ the surface morphology at temperature above 1000 °C (which we will call high temperatures) with sub-nanometer vertical resolution (which would allow the direct observation of atomic steps) are low energy electron microscopy (LEEM) [42-44] and, to a certain extent, reflection electron microscopy (REM) [45-47]. Even these methods have a reduced applicability when the surface premelts or roughens. For this reason, in order to observe the surface structure using methods such as AFM or scanning tunneling microscopy (STM), only quenched (low temperature) samples can be used. But quenching in UHV is not a very effective way to completely freeze in the morphology of a high temperature surface due to the relatively high density of atomic steps present on vicinal surfaces. These steps, usually only a few thousands Ås apart, act during quenching as a high density network of sinks for the atoms forming the nonequilibrium features. As a result it is very difficult to preserve the high temperatures features on a regular, stepped surface, even when the miscut angle of the starting wafer is very small (~ 0.1°).

To address this issue we used our specially prepared surfaces on which large step-free regions were obtained as described above. Moreover, in order to investigate the changes that occur on the surface close to the phase transitions temperature we also used nonuniform heated samples so that a continuous range of temperatures could be probed. In this way, we are able to report surface morphologies observed on the

silicon surfaces that we will explain as signatures of high temperature surface phase transitions such as incomplete surface melting and (1×1) → (7×7) reconstruction. We would like to highlight in advance that some qualitatively similar structures appeared in earlier papers (without being discussed in detail) when the step bunching generated microns wide terraces (for example [4, 48, 49]).

In chapter 2 we will concentrate on the following issues that we consider are not yet fully understood:

- How the premelting of the Si(111) surface occurs (where the first nuclei of molten silicon form, how the molten phase evolve, what are the implications of having large atomically flat surfaces)?
- What is the Si(111) surface morphology at increasingly high temperature (close to the bulk melting temperature)?
- Is there a surface premelting on Si(001)?
- What are the morphological consequences of (1×1) → (7×7) transition on Si(111) if surface features, remnants of surface premelting, still persist at around 850 °C in certain surface regions?

Even though the "mirror polished" surface of a commercial CZ silicon wafer has a very small measured roughness, the chemical mechanical polishing procedure does not generate a thermodynamically stable surface. Atomic steps cannot be detected even using STM (see for example Refs. [27, 50]). Furthermore, the reactive ion etching (RIE) used in patterning is known to further increase the roughness (see for example [51, 52]). Only after an extended high temperature anneal and a rather slow cooling period do atomic step and terrace structures become visible. While the effect of the UHV high temperature annealing on the flow characteristics of pre-existing step arrays has been extensively studied, much less is known about how the surface transform from the rather disordered initial state to the final step and flat

terrace state. Furthermore it is usually assumed that the roughness decreases monotonically upon annealing [18, 21, 24]; as shown below, this is not always the case.

Obtaining atomically flat surface regions is not only useful for basic science studies but may be desirable for silicon microelectronics since the dimensions of CMOS transistors are in the sub-100nm regime; the gate oxide thickness for example, has already reached the practical limit (~1.2 nm SiO_2) since any reduction beyond this would result in massive increases in leakage currents. Even after the pending introduction of high-K dielectrics [53, 54], good dielectric uniformity and a smooth dielectric-semiconductor interface will still be desirable for any further scaling down and for reducing charge carrier scattering at this interface. In addition, the continuous reduction in feature size makes the removal of the heat generated by this leakage current more and more difficult. Controlling the surface morphology (shape and smoothness) will be even more important for future nonplanar transistors such as multi-gate field effect transistors (see for example Hiramoto [55], Lin and Sze [56] and references therein). Several recent papers have described the changes in the morphology of trench sidewalls etched into Si(001) under high temperature hydrogen anneal [21, 22, 57].

In chapter 3 we follow the evolution of the morphology of vicinal Si(111) surfaces during UHV annealing in details for two types of surface regions: (i) general flat areas of the surface (evolution of surface roughness as a function of annealing temperature) and (ii) near the edges of patterned structures such as craters and mesas (trenches and ridges development).

In the last chapter (chapter 4) we report results related to two applications using our substrates processed by UHV high temperature annealing.

As CMOS transistors are scaled down various issues have to be overcome in order to increase the performance of integrated circuits (see for example [58]). Among these, and often overlooked, is the quality of the interface between the gate oxide and silicon channel. The roughness of this interface generates carrier scattering (thus reducing the channel mobility [59]) and current losses through dielectric tunneling. At oxide thicknesses below 3 nm, even atomic steps represent defects that can considerably reduce the effective oxide thickness [60]. To investigate the influence of surface roughness we have built MOS capacitors on three types of silicon surfaces (see also Fig. 1.2): atomically flat surfaces, normal (stepped) surfaces cleaned in UHV by high-temperature annealing, and normal, RCA cleaned wafer surfaces (Chap. 4.1).

In another application (Chap. 4.2), Si(111) substrates with regular arrays of atomic steps were used to induce azimuthal alignment of crystals in thin polycrystalline pentacene films. Pentacene (Fig. 1.4) is a promising organic semiconductor being studied as a candidate for inexpensive, large-area organic-based electronics. One of the main challenges is to obtain a much higher mobility of the charge carriers in the pentacene film, since, due to the its polycrystalline structure, there are a lot of scattering processes taking place at high angle grain boundaries.

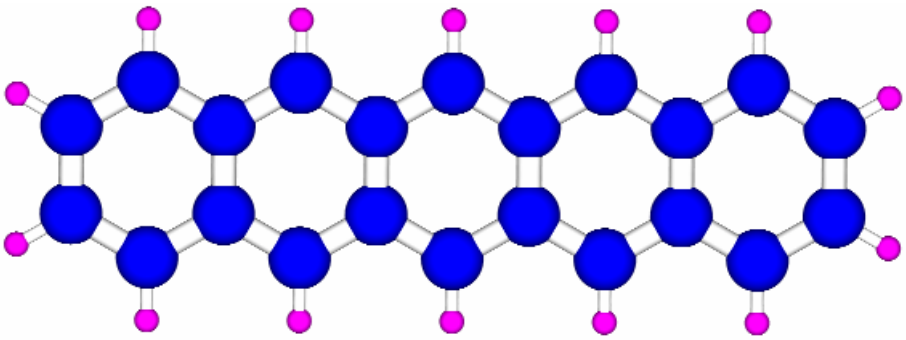

Figure1.4. Schematic of the pentacene molecular structure; bigger spheres are carbon atoms and smaller ones are hydrogen atoms.

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CHAPTER 2

NOVEL SURFACE MORPHOLOGIES RELATED TO SURFACE PREMELTING AND TO (1×1) → (7×7) PHASE TRANSITIONS

In this chapter we report what we believe to be the first morphological evidence for the occurrence of surface pre-melting on the Si(111) surface. Our results complement the extensive previous evidence from diffraction and ion scattering techniques for the presence of pre-melted (liquid-like) layers on Si(111) below the bulk melting temperature and also suggest how atomic steps are involved in the initiation of such layers. Our results are based on AFM studies of morphologies that are preserved when surfaces are annealed in a range of high temperatures and then rapidly cooled to room temperature for observation. A unique feature of the experiments is the use of specially prepared atomically flat or very low step density surfaces; this allows us to see how the liquid-like morphologies are associated with the steps and also allows the high temperature structures to survive the cooling process without being absorbed into the steps which normally would exist on a surface vicinal to (111). We also show that quenched-in structures ascribed to pre-melting can act as sinks for diffusing 'excess' adatoms generated by the (1×1) to (7×7) transition at much lower temperature.

2.1 Overview of surface melting and roughening

2.1.1 Thermodynamic and kinetic considerations

As the temperature of a crystalline material approaches its melting temperature (T_m), the surface could start to disorder even though the bulk of the crystal remains mostly unchanged. The phenomenon of surface melting below the bulk melting temperature is called surface (or interfacial) premelting (see for example the reviews [1-4]). From energy consideration, a surface starts to melts when the sum of the surface tension of the liquid-vapor, γ_{LV} and liquid-solid interfaces, γ_{SL} becomes lower than the surface tension of the solid-vapor interface, γ_{SV} (for example [5]).

$$\gamma_{LV} + \gamma_{SL} < \gamma_{SV} \tag{2.1}$$

While the above relation (2.1) is a necessary condition for a surface to premelt, it is not a sufficient one. One case in which a surface can remain "dry", even though it is more thermodynamically favorable to have a "wet" one, is when the surface is not in equilibrium with its vapors. In fact the experimental conditions in which most of the high temperature surface studies take place there is no equilibrium between the material surface (being it in the solid or liquid phase) and its vapors. In UHV the vapor pressure is a rather meaningless concept as practically all the atoms that leave the surface will not return to it. Therefore the kinetic effects (i.e. the rate of sublimation/evaporation) could change the surface melting characteristics. More precisely, if the rate of evaporation $\mathcal{R}_{LV}$ is higher than the rate of atoms going from the solid to liquid phase $\mathcal{R}_{SL,}$, $\mathcal{R}_{LV} > \mathcal{R}_{SL}$, then there will be no molten layer on the surface even though the relation (1) still holds (see Fig. 2.1), i.e. the onset of premelting would be delayed. An elegant way of obtaining the true thermodynamic equilibrium is to use two parallel heated samples with only a small gap between their active surfaces [6, 7].

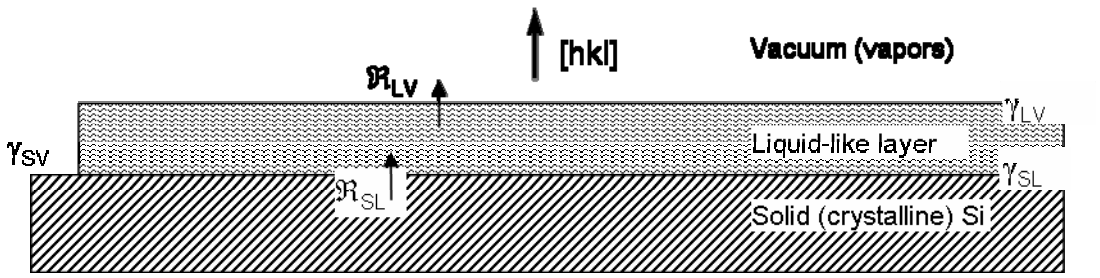

Figure 2.1. Diagram of a [hkl] oriented crystalline Si surface covered by a molten layer. In case of non-equilibrium conditions (~ zero vapor pressure), the existence of a molten layer requires $\Re_{LV} < \Re_{SL}$. Experiments showed that this condition is fulfilled for Si(111) from the onset of surface premelting up to the bulk melting point. $\Re_{IJ}$ represent the exchange rate and γ_{IJ} represent the interface energy between I and J phase respectively; I, J can be solid (S), liquid (L), vapor (V).

In order to effectively use the relation (2.1) for predicting which surface orientation would melt, we need the accurate values of surface tension γ_{LV}, γ_{SL}, and γ_{SV} and their temperature dependence for at least several low index crystallographic orientations. This values are highly sensitive to surface reconstruction (γ_{SV}), background gas pressure (γ_{LV}) and surface contamination (γ_{SV}, γ_{SL}) For example, taking the Si(111) case into consideration, we found the following experimental values for surface energies:

- γ_{SV} ~ 1.25 J/m^2 for cleaved silicon samples at liquid nitrogen temperature [8, 9]; cleaved Si(111) surfaces are known to reconstruct into a metastable (2x1) structure, for which the theoretical calculations predict a surface energy of around 1.4 J/m^2 ([10] and the related references therein). If we assume that close to the bulk melting temperature the silicon surface tension values should be close to the unreconstructed 1x1, the calculated values for this relaxed surface is about 1.75 J/m^2 [10]

- $\gamma_{LV} \sim 0.8$ J/m^2 at bulk melting point [11]
- $\gamma_{SL} \sim 0.65$ J/m^2 at bulk melting point (but $\gamma_{SL} \sim 0.6$ J/m^2 at 1200 °C) [12]

Using these values one can see that close to the bulk melting temperature, the relation (2.1) is satisfied (if we take $\gamma_{SV} = 1.75$ J/m^2, or any value higher than 1.45 J/m^2). Extending now the same reasoning for the other surface orientations and recognizing that the (111) crystallographic direction has the lowest energy for silicon [6, 13], according to the relation (2.1) all the other silicon surface orientation should undergo surface premelting at even lower temperatures than Si(111) (γ_{LV} is isotropic and γ_{SL} should only have a smaller anisotropy with the surface orientation compared to γ_{SV}).

One way the melting of a solid material could progress is when the thickness of the disordered layer at the surface increases continuously. This process is commonly known as complete surface melting. There are situations when the thickness of the disordered surface layer remains finite at the triple point. This phase transition is called incomplete surface melting [14]. The effect is due to a delicate balance between the adhesion forces between the solid and its molten layer and the cohesion of this liquid layer [15, 16].

In Fig. 2.2 we show the effect of the occurrence of partial surface melting on the pressure-temperature equilibrium diagram (a somewhat similar diagram was published by Nenow in his review on surface premelting [1]). As one can see, for each molten layer the system has a slightly different triple point. At highest temperature one can recover the classical triple point corresponding to the equilibrium between solid, liquid and vapor phase. Again we have to recall that the equilibrium conditions are rather the exception than the rule in UHV systems, therefore our system at high temperature is not really crossing the solid-liquid coexistence line, but the effect on the bulk melting temperature is not significant. For qualitative phase diagram of silicon one can consult the Refs. [17-19].

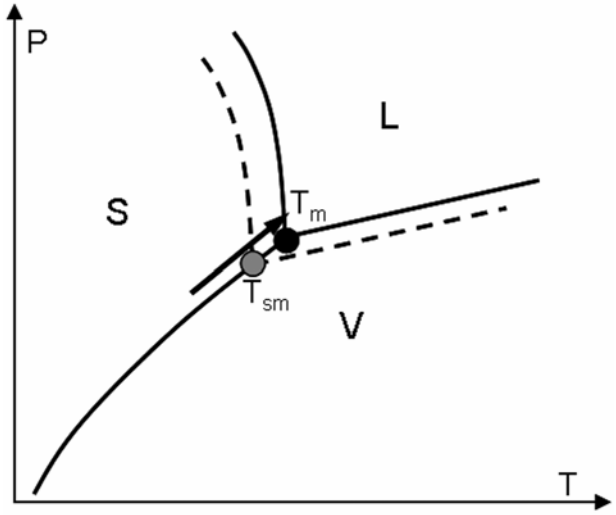

Figure 2.2. Pressure (P) vs. temperature (T) equilibrium phase diagram in the case of a solid that undergoes surface premelting (notice the negative slope of the solid – liquid coexistence line characteristics to silicon). T_m is the bulk melting temperature corresponding to the triple point and T_{sm} is the temperature (on the solid-liquid coexistence curve) at which the first layer melts. If subsequent layers disorder, there will be a sequence $T_{sm1} < T_{sm2} < \ldots < T_m$

A reversible melting transition of the surface of a three dimensional crystal was first observed by Frenken and van der Veen on atomically clean Pb(110) surface using ion scattering measurements [20]. The first experimental evidence of surface premelting on semiconductors came from the low energy electron diffraction (LEED) study of Ge(111) surface, where, at 150 °C below germanium bulk melting temperature, the nonspecular LEED spots weaken substantially as a result of loss of crystalline order at the surface without any broadening of the specular beam as would happen if the surface roughened [21]. For simplicity, throughout this article we will use the term surface melting for the incomplete surface melting.

The surface melting is often confused with surface roughening and both occur often a few hundred degrees below the melting temperature. The origin of transitions

towards a disordered surface is related in both cases to the fact that the atoms within the topmost layer of the crystal are less bonded and therefore the thermal disorder have a higher impact on the atoms at the boundaries. According to the terrace-ledge-kink model with a simple cubic atom approximation, the ratio of binding energies of atoms on unreconstructed (111) terraces to that of the bulk is 5/6, hinting that a terrace melting is possible at a temperature $T_{sm} = 5/6\ T_m$ (T_{sm} being the temperature of the onset of surface melting and T_m being the bulk melting temperature on an absolute scale) [22]. Applying this rule to the Si(111) surface would result in a surface disordering temperature of ~ 1130 °C. For unreconstructed Si(001) the surface melting should occur at $T_{sm} = 3/4\ T_m$ (990 °C), but at this temperature the (2x1) reconstruction is still in place. Adding the result of this estimation to the fact that the reconstruction reduces the Si(001) surface energy by a sizable 1.7 eV per dimer [23], we can understand that the de-reconstruction of this surface, even a partial one, would have a big impact on the behavior of Si(001) at high temperatures.

During roughening transition the step free energy becomes zero and accordingly, an arbitrarily large number of steps can nucleate on the surface resulting in a delocalized interface between solid and its vapors (for example [24]). Mathematically this property can be defined as the divergence of the height correlation function, the macroscopic effect of the roughening transition being that the corresponding facet disappears on the 3D equilibrium shape. The thickness of the disordered layer increases with temperature and diverges at T_m [25]. This is the so called Kosterlitz-Thouless roughening and its driving force is of thermodynamic origin. The mathematical model that describes this transition is called solid on solid (SOS) and it is formally equivalent to the Ising model (see for example the reviews [26-28]). Mostly from epitaxial deposition studies, another type of roughening, kinetic roughening is known to be caused by nonequilibrium conditions at the surface (see for

example [29]). The process of kinetic roughening is also important at high temperatures where an intense sublimation of atoms from the surface generates non-equilibrium conditions for short range structural disorder (adatom-vacancy pairs, pits formed by the vacancy clustering, etc.).

Whilst in the case of roughening the surfaces maintain lateral order but loose the vertical order [30], the surface molten layer is believed to be a flat quasi-liquid [31, 32], for which the crystallinity has disappeared in the second and third neighbor shell of the in-plane correlation function [33], while some local periodicity is imposed by the crystalline underlying substrate. The diffusivity of adatoms increase greatly [34, 35] as the topmost layer becomes liquid-like (almost zero shear modulus [36] and liquid-like diffusion constant [34]). But because only one or a few top layers melt, atomic steps remain well defined as the underneath material remains flat and crystalline. However, it is possible that in some particular cases the distinction between surface melting and surface roughening is mostly theoretical, i.e. the roughening transition could trigger a surface melting (eventually a complete surface melting), or the roughening transition could take place at the interface of crystal wetted in its own liquid. In this latter case it was shown that the presence of a thin liquid film would hinder the roughening at least until the molten layer becomes so thick (near the bulk melting point) that the two interfaces decouples [37].

It was observed that in some metals, such as Al(110), the surface roughens at much lower temperature than it melts (see for example ref. [38]). Di Tolla et al. [39] also suggested that surface melting should precede the roughening transition but they recognized that some surfaces, such as Pb(111) [40-42], do not roughen or melt up to the melting point. In fact fast laser local heated Pb(111) surfaces are known to remain crystalline even at temperatures higher than the bulk melting point [43, 44]. But even in this case there are a few reports that a certain degree of disorder appears on the

Pb(111) surface near the bulk melting point [45, 46] (which could be caused by the miscut of the (111) plane).

Despite the continuous efforts to develop predictable theories on roughening and surface melting [47-55], no complete model is known to predict for which materials, surface orientations or at which temperatures certain type of surface disorder would occur. This difficulty arises also from the fact that roughening transition is a long range perturbation of the surface morphology, while the formation of a liquid-like layer involves changes in the short range order of the surface atoms [56]. The only work we are aware of that connects these two apparent distinct phenomena was proposed by Jagla and Tossati [57, 58]. Using a 3D N-state lattice Potts model, the authors have shown that a pre-roughening transition (which appears in SOS models if interactions of longer range than nearest-neighbor are considered) can be induced by the onset of the surface melting. A recent review that summarizes the state of the theoretical knowledge in the field of surface melting was published by Tartaglino et al. [59].

2.1.2 Surface premelting on Si(111)

Clean Si(111) vicinal surface does not undergo a thermodynamic roughening transition up to the silicon melting temperature. In fact, in most cases of fcc materials, the densely packed crystallographic plane, such as (111), do not roughen up to the bulk melting temperature [29]. Natori and Harada calculated the step free energy and observed that it does not change significantly with temperature up to the surface melting temperature, implying that surface melting occurs at a temperature lower than the eventual roughening transition on Si(111) [60]. The experiments performed by Heyraud et al. [61] indeed showed that the Si(111) surface does not become rough up

to 1400 °C, therefore the roughening transition is not a prerequisite for the surface melting.

The surface melting on Si(111) was analyzed theoretically [60, 62] and in situ through experiments using X-ray core-level photoemission [63], helium atom scattering [64], medium-energy ion scattering (MEIS) [25, 65], and reflection high-energy electron diffraction (RHEED) [22, 25, 66-68]. Other experiments were done on quenched samples using UHV scanning electron microscopy (SEM) [69-72]. With the exception of the work of Homma et al. [69-72], all the studies were performed on vicinal silicon surfaces characterized by a relatively high step density.

The temperature at which the Si(111) surface melting occurs is reported to be within 1200 – 1300 °C range. One explanation of this rather broad span could be related to the difficulties in accurately measure the temperature of the annealed samples inside the UHV chambers. Almost all the experiments are done using DC heating and non-perfect sample clamping to the sample holder accounts for temperature gradients across the sample therefore limiting the accuracy of the calibration through the melting point. Moreover, the Monte-Carlo simulations performed by Natori et al. using empirical Tersoff-Dodson potential suggested that the stress induced in the samples can also explain some differences in the surface melting temperature [73]. Previously, similar simulations showed that a higher miscut angle of the Si(111) surface decreases the transition temperature as expected because the surface melting seems to start from the upper edge of a step, at least if the adatom coverage is low enough [60]. Finally there are experimental evidences that dopants could also influence the temperature of surface melting transition. For example Homma et al. observed that surface melting occurred at 1260 °C for samples obtained from Si(111) heavily boron doped (~0.001 Ω-cm) 0.3° miscut wafers, but it happened at 1200 °C for samples obtained from lightly boron doped (~5 Ω-cm) 0.15° miscut

wafers [71, 72]. The observation that the boron increases T_{sm} is somewhat counterintuitive because the according to the Si-B constitutional phase diagram [74], a Si-B alloy with less than 0.1 atomic fraction B should melt at lower temperature than pure silicon. We do observe on highly B doped samples much rougher steps and more bi-layer deep surface pits that could be explained by a faster sublimation of B-enriched surface regions. An increase in the evaporation rate could possibly delay the onset of surface melting in this case.

2.1.3 Surface disordering at high temperatures on Si(001)

At room temperature the clean Si(001) surfaces reconstruct forming alternative (1x2) – (2x1) domains. The (2x1) reconstruction of the Si(001) survives at least up to the roughening transition [6, 75] (~1200 °C). There are experimental evidences that the Si(001) surface acquire a metallic nature starting at 630 °C, but this behavior is not caused by the dimer break-up and it was explained by the fast dimer flipping at high temperature [76, 77] and latter by transformation of dimer structure from asymmetric to a symmetric configuration [78, 79].

The (2x1) reconstruction of the Si(001) surface was first inferred from the low energy electron diffraction (LEED) patterns by Schlier and Farnsworth [80] and was directly revealed using scanning tunneling microscopy (STM) by Hamers et. al [82].

The existence of surface melting phase transition in the case of Si(001) is still controversial. First of all the (2x1) surface reconstruction should break before the onset of the surface melting. Secondly, it is considered that dimer breaking is related to the surface roughening as the unreconstructed (001) surface is not a stable facet [6]. The roughening transition on Si(001) was predicted by Monte Carlo simulations by Salanon et al. [82] and was confirmed by various experiments [83-86]. Metois and

Wolf [83] observed that while below 1160 °C the sublimation takes place by step-flow, above this temperature, holes of monoatomic depth form on the terraces. At even higher temperature the steps proliferates at the surface and the vicinal surface with well defined steps is destroyed. The authors concluded that Si(001) underwent a kinetic roughening. The STM investigations presented in Ref. [85] revealed that the normalized terrace length distribution of 4° misoriented Si(001) surfaces bore the characteristics of a rough surface, but the height-height correlation function did not diverge logarithmic as expected for the roughening transition. By extrapolating the step stiffness, Bartelt et al. [84, 86] showed that step energies go to zero as the roughening temperature is approached (~1200 °C). The authors concluded that the roughening on the Si(001) is thermodynamic and not due to the onset of sublimation (see also Refs. [87, 88]).

In a molecular dynamics simulations using the effective-medium tight-binding model has been found that in the presence of a high concentration of vacancies (25%) the Si(001) undergoes a phase transition at 1280 °C, where the first layers melt and form a liquid state [89]. There are also several experiments where the observed disorder that take place on the Si(001) surface was attributed to the surface melting. Fraxedas et al. observed by high-energy photoelectron diffraction a phase transition at about 1130 °C that they interpreted as a surface melting, with a stable thickness of the liquid film of two atomic layers [90]. The RHEED studies of the Si(001) revealed a lack of order at the crystal surface above 1130 °C, which again was attributed to an incomplete surface melting [91]. In a parallel experiment that confirmed the surface melting on Si(111) at 1200 °C, MEIS measurements also exposed the appearance of a disordered layer at 1250 °C, but its thickness varied continuously with temperature (~ 4ML at 1360 °C) [65]. X-ray absorption and valence band spectroscopy studies revealed a sudden and significant increase in the metallicity of Si(001) surface at 1340

°C that could be a mark of a surface melting phase transition [75, 92], while a sign of possible break up of the dimer reconstruction has been detected at 1210 °C [75]. Kimura and Itari from the in situ observations of synchrotron X-ray reflectivity [93] concluded that Si(001) undergoes surface melting between 1200 °C – 1300 °C and this transition is reversible. The density of the surface changed from 2.3 g/cm^3 to 2.5 g/cm^3, which correspond approximately to the silicon density in the bulk and liquid states respectively (for some properties of bulk and liquid Si see for example [94] and references therein). When heated above 1350 °C, the surface roughened irreversibly. The experiment was performed in He atmosphere at rather high pressure (2 Torr) and in this case the effective vapor pressure of silicon was relatively close to its equilibrium value.

2.2 Surface structures associated with surface premelting

2.2.1 The case of Si(111) surface

In the Figs. 2.3 – 2.5 we present surface structures that are relevant for uncovering novel characteristics of the onset of surface melting. The annealing temperature in the region we obtained these images is about 1200 °C. Similar structures were only found in an area on the sample of ~1 × 0.5 mm, where the temperature was very close to (but above) the surface melting transition. The temperature in this region varied only by ± 5 °C. The separation between this region of the sample where this kind of surface structures are present and the surrounding areas is smooth, meaning that smaller and smaller features as seen in Figs. 2.3–2.5 can be detected towards the limits of this region.

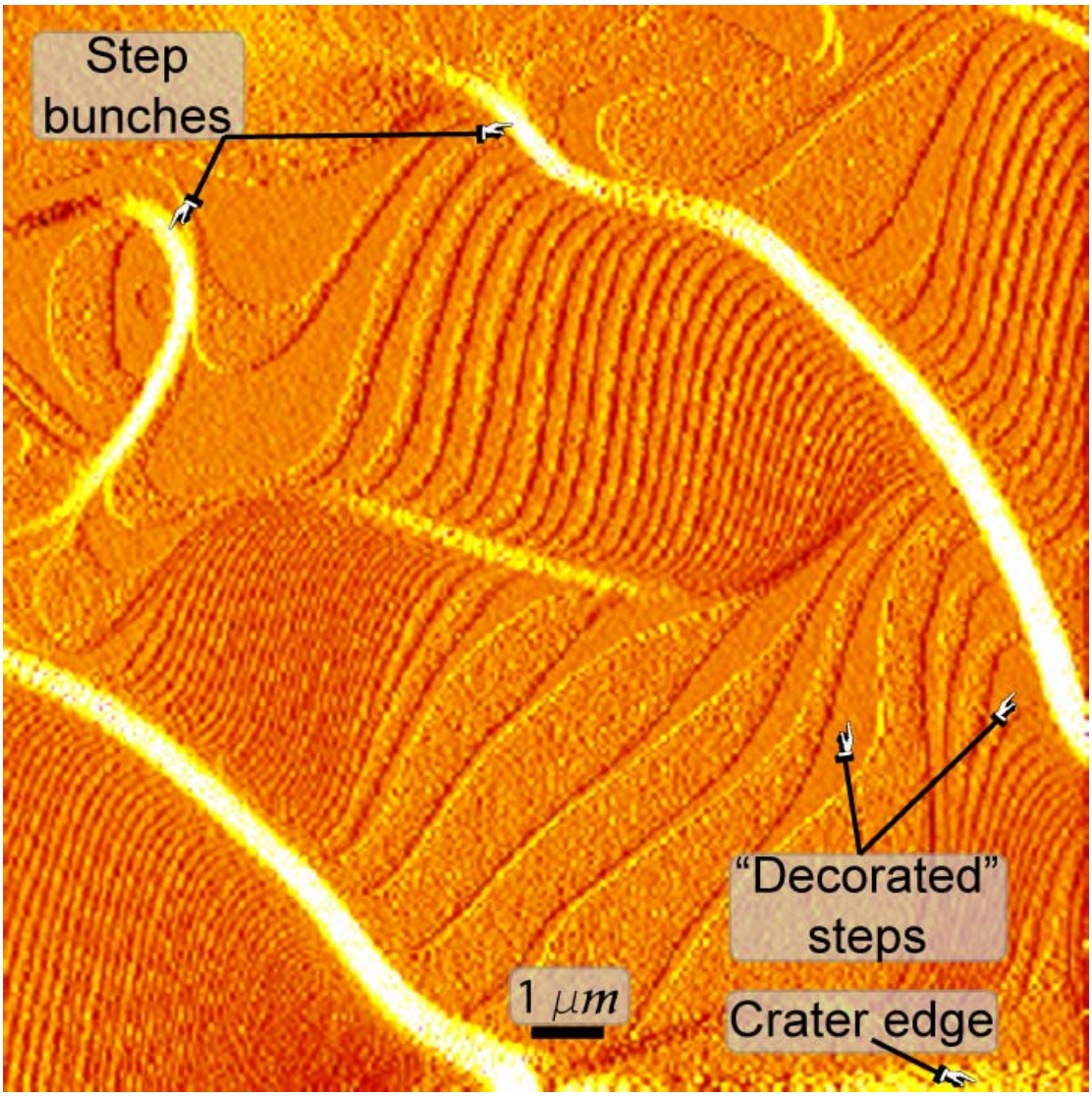

Figure 2.3. AFM scan (derivative mode) showing two step bunches with other islands running perpendicular to these bunches; most of the step edges are decorated with bands of adatoms. The edge contrast is enhanced by using the height derivative (amplitude); white edges means step-up, dark edges means step down.

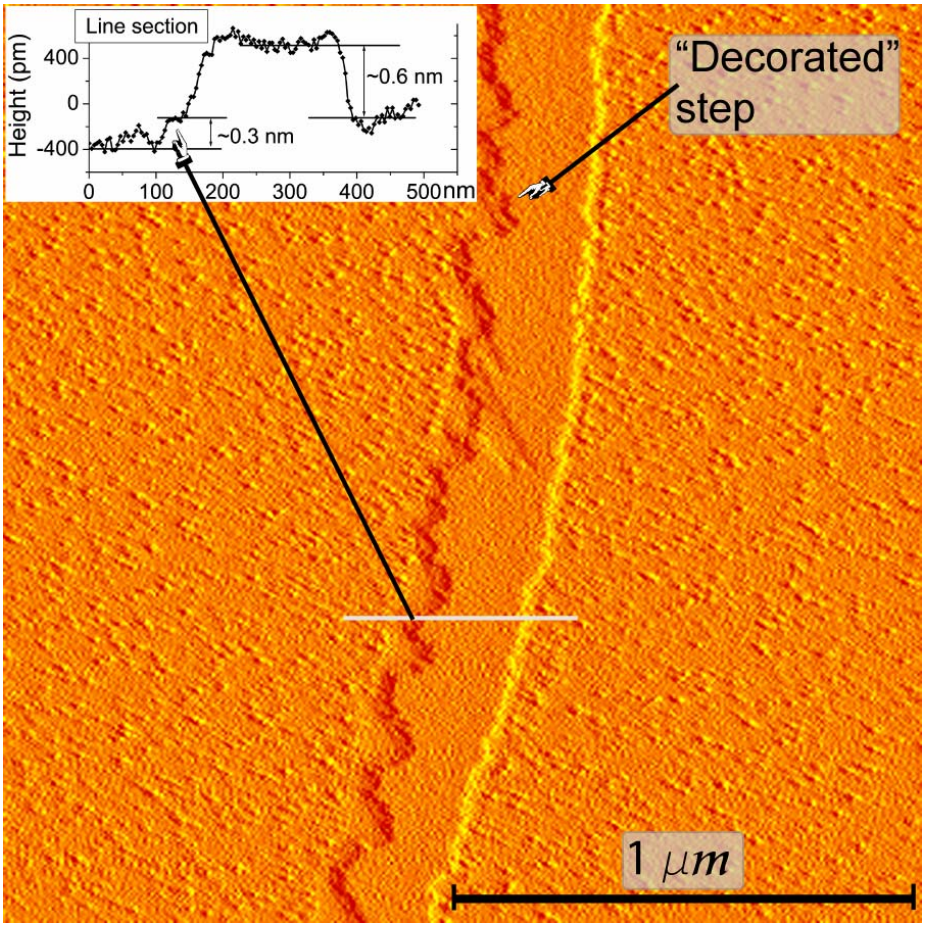

Figure 2.4. Line section across a decorated step; the underlying step can be seen in certain regions of the vertical band (see the kink pointed by an arrow in the line section).

Figure 2.3 shows an AFM image taken on a stepped area, outside of the patterned region. In between step bunches one can observe a rather regular array of wavy, elongated islands. A line section performed over such an island (Fig. 2.4) shows that its height is three atomic interplanar distances (~ 0.9 nm) on the one side (left side in the case shown in Fig. 2.4) and two interplanar distances (~0.6 nm) on the opposite side of the island (right side in Fig. 2.4). This morphology tells us that these islands are placed in the regions where an upper and a lower terrace intersect forming an atomic step. In fact the underlying step can be observed in Fig. 2.4 as a small kink

~0.3 nm in height at the left side of the elevated structure that resides on the upper terrace. The many small islands seen on the terraces are a result of adatoms clustering during the quenching. By comparison, the top surface of the elongated islands is rather smooth.

We propose the following explanation for the formation of such bands at the upper terrace of atomic steps. It is expected that the surface melting to nucleate at the step edges, where the atoms are weaker bounded. At a temperature slightly below the onset of surface melting, sub-critical nuclei randomly form at the step edges (most likely at the upper terraces), but they disappear either by evaporation, either by breaking up into clusters of more or less ordered adatoms. This stage is probably related to the precursor of surface melting as described in the Refs. [64, 67, 68]. The surface maintains overall its crystallinity and no major changes in the surface morphology are expected to be seen on the quenched samples. At a slightly higher temperature the molten nuclei are able to grow above a critical size and these quasi-liquid regions coalesce and start to spread over the surface, starting from step edges. We have to keep in mind that the step flow is prevalent at this temperature (~1200 °C). The fact that the molten layer becomes pilled-up at the upper-terrace side of the retracting underlying crystalline steps proves that there has to be a rather strong ES barrier for the atoms at the upper terrace to be gathered into a two bilayer thick structure (correlated with a relatively high viscosity of the disordered layer). We will refer to these structures probably formed by “shoveling” of the molten layer by the moving crystalline steps as decorated steps. Obviously the structure formed in this way cannot be wider than the distance to the next atomic step. Indeed if the step density is too high, these structures will not survive during quenching as seen in the left-lower corner of Fig. 2.3, where only simple atomic steps can be distinguished.

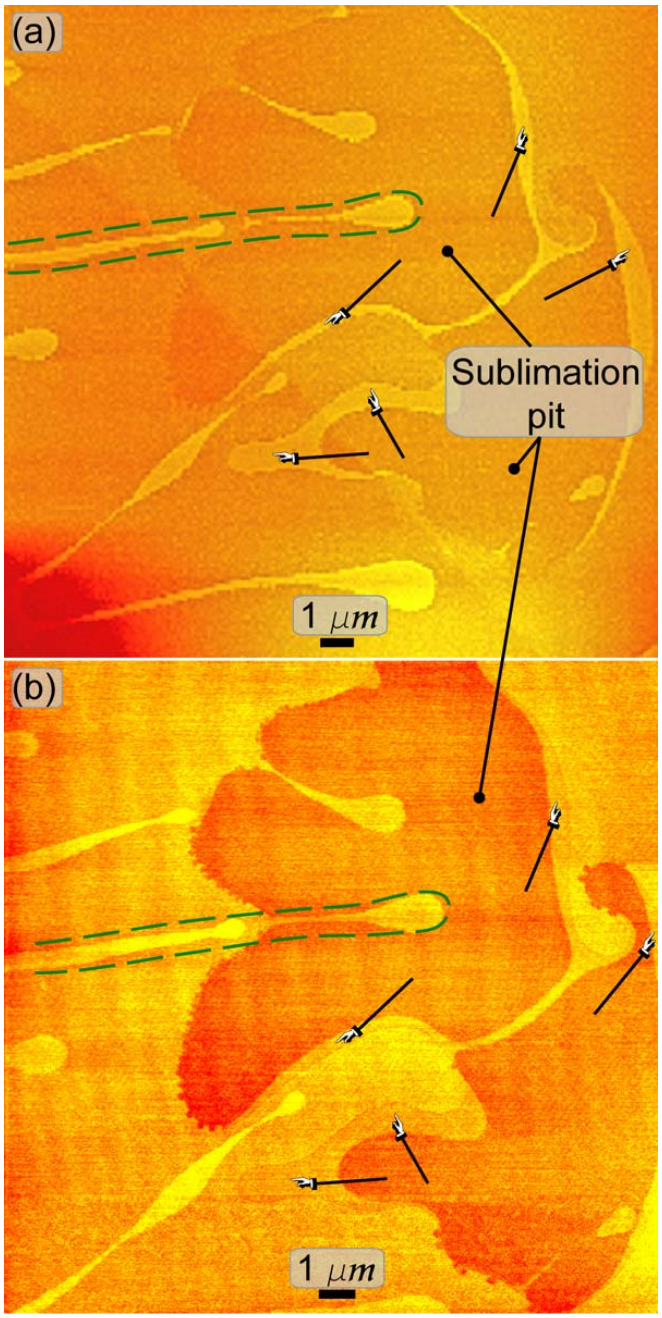

Figure 2.5. (a) AFM image revealing liquid-like elongated islands. The right side of the inner crater is also decorated. The dashed line suggests the possible shape of a molten structure before quenching. (b) The same region imaged as in Fig. 2.5(a), but after the sample was chemically cleaned (etched) following the standard RCA procedure. The step decoration was selectively removed demonstrating that these structures were not fully crystalline regions. Notice the jagged edges in the regions that were not covered by the molten structures.

The AFM shown in Fig. 2.5 (a) reveals similar decorated islands especially at the right side of the pit, which formed due to the coalesce of vacancies [72]. The image was taken at the bottom of a crater where the step flow generated a nearly step free region. The direction of the electric field in this case is from the left to the right and it is known that the the atoms in the molten layer for Si(111) have a positive effective charge [95-98]. The fact that the step decoration is present preferentially at the the right edge of the pit provides evidence that the electromigration enhances the Ehrlich – Schwoebel (ES) barrier, while on the left side the electromigration reduces the ES barrier allowing the atoms from the top terrace to be incorporated in the step.

The most striking characteristics of the surface morphology shown in Fig. 2.5(a) is the presence on liquid-like, long islands that runs mostly from the left to the right. The height of these islands is ~0.6 nm (two bi-layers). They originate either from the left crater wall, or from the left edge of the pit formed on the lowest region in the upper-right part of the crater and are running from the left to the right (the direction of electric current), hinting that electromigration played an important role in their formation and maintenance. We can assume that although these long islands seen in the Fig. 2.5 reflect the morphology of the surface after the onset of the surface melting, a certain degree of dewetting (shrinking) definitely took place during quenching. This can be understood by realizing that some of the features seen in Fig. 2.5 look like they broke apart during quenching. The morphology of the molten islands spreading on an atomically flat surface (before quenching) might look like the dashed line drawn in Fig. 2.5(a).

The key aspect that explains the presence of these long islands is that in the absence of atomic steps or other extended defects, the occurrence of surface melting is hindered. Therefore, even though from energetic reasons the appearance of a molten layer is favored (see Eq. 2.1), due to the lack of sites for nucleation, the atomically flat

regions at the bottom of the craters maintains their crystallinity up to a higher temperature. However the crater is limited by crater walls that consist in high index crystallographic planes. It is well known that the high index surface orientation disorder at much lower temperatures. In fact many of the high index planes, with the notable exception of Si(113) (which starts to disorder at 680 °C [99-101], but seems to roughen at around 1330 °C [61]) undergo surface disordering at temperatures in the range 750 – 900 °C [102]. The disordering of the high index plane surface at lower temperatures is expected due to the anisotropy of the surface free energy [13]. At around 1200 °C the rate with which the high index planes that forms the crater's walls disorder is probably higher than the local sublimation rate which results in a net flux of adatoms from the crater's wall towards its flat bottom. As the flat terrace does not reach yet the overheating needed for the onset the surface melting (in the absence of atomic steps), these adatoms cluster at the bottom of the crater near its walls in a liquid-like layer. The electromigration tends to push these clusters further inside the almost step-free region (see the anisotropy in the orientation of the elongated islands in Fig. 2.5). Because there is not enough supply of adatoms to fill in a full liquid layer, the adatoms are channeled in finger-like protrusions. The molten protrusions advancing on the flat crystalline crater's bottom reduce the local free energy of the surface, hence the relatively strong attraction between the overheated crystalline surface and the quasi-liquid layer probably also accounts for the dynamical stability of these features. A more detailed inspection of the region at the border of the craters' bottom, revealed that this kind of protrusions forms starting from all walls, but only those that are favored by the electromigration effect grow to appreciable sizes. We would like to notice that the presence of the protrusions near the high index plane structure on Si(111) surface (but smaller ones) can also be seen at a careful inspection in other published papers (see for example Fig. 2(b) from Ref. [103]).

It is somewhat surprising that both types of the liquid-like structures (decorated steps and protrusions) are two (or three) bi-layers thick, especially if we recall that the experiments performed on the Si(111) surface melting showed that a single atomic layer of liquid is present up to the bulk melting temperature.

It is expected that a certain degree of layering is present if the liquid layer is two atomic layers thick, with the layer closer to the crystalline interface having a higher degree of order. Upon quenching, the first liquid layer could easily regain its crystallinity, while the second liquid layer would transform into a "frozen" amorphous-like, loosely bonded clusters of atoms. In order to test the difference in the crystallinity of these structures, we performed an RCA cleaning, which is known to slowly etch the thin oxide layer on silicon and to continuously grow a conformal new oxide layer by re-oxidation. After the RCA cleaning, the strips that decorated the upper edge of the steps were etched away faster than the underlying crystalline surface and disappeared from the surface, while the shape of the elongated protrusions was fully preserved, but their remaining height was only one bi-layer. The resulting surface morphology, as seen in Fig. 2.5(b), reveals the atomic steps that existed underneath those bands. We can conclude that there is a marked difference between the degrees of crystallinity of the first bi-layer of the quenched liquid-like structures compared to the second (eventually third) layer that was completely etched away

At temperatures higher than 1220 °C, the surface melting spreads over most of the surface, including over the step-free regions. As a result, none of the features described above are preserved as they are included in the molten layer and the AFM images taken on the substrates heated at temperatures higher than 1220 °C reveal after quenching a normal flat surface, without any liquid-like structures.

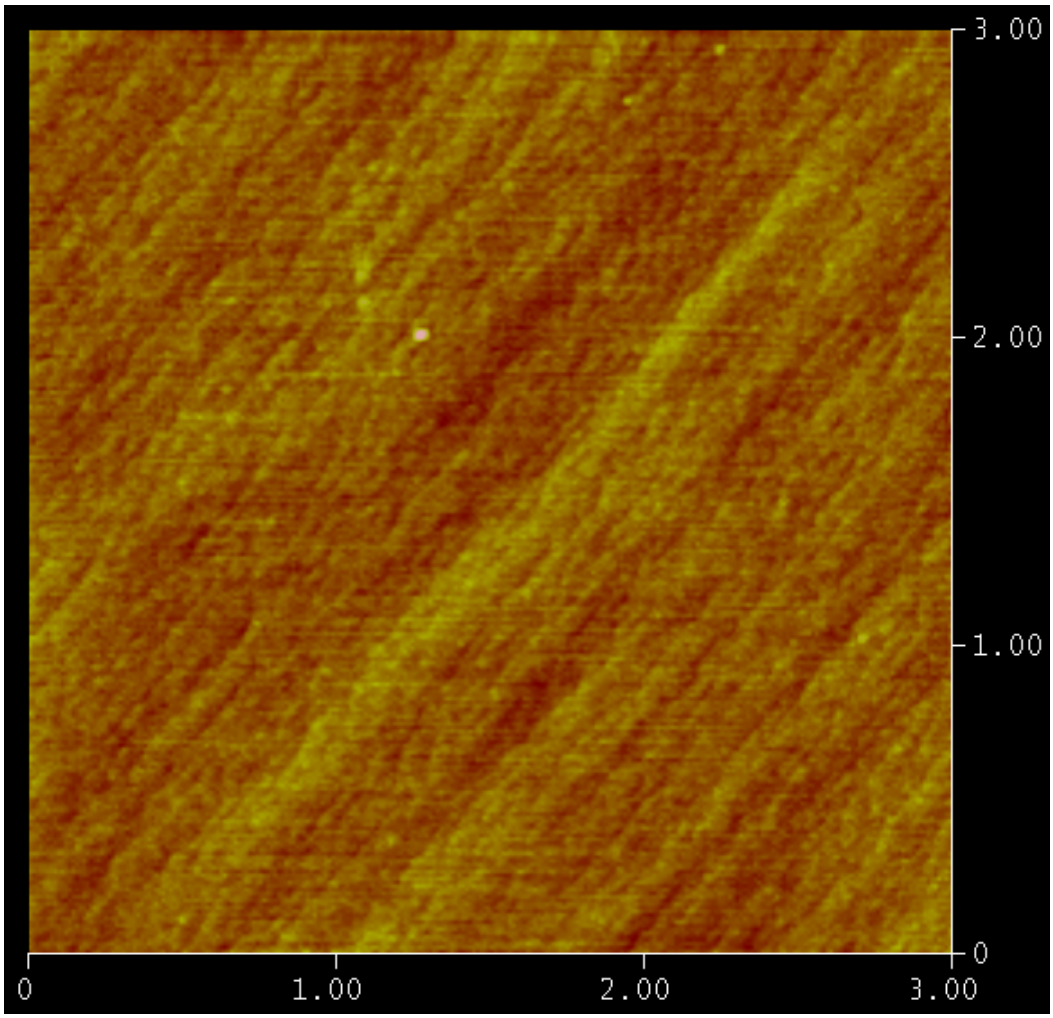

Figure 2.6. Barely visible atomic steps on a sample quenched from about 1330 °C (3×3 μm AFM scan).

The samples quenched from temperatures higher than 1300 °C show increasingly fuzzy steps (Fig. 2.6; see also Fig. 1(d) from Ref. [104]) and on those quenched from above 1360 °C the steps can no longer be imaged by AFM. The fact that the atomic steps are well defined if the samples where quenched from ~ 1250 °C, but become fuzzy when the quenching temperature was raised above 1300 °C can be explained by taking into account the degree of order in the molten layer and into the

crystalline substrate underneath. More precisely, at around 1250 °C, the quasi-liquid layer still maintain a rather high degree of order imposed also by the well ordered underlying crystalline substrate. During quenching, this local order within the molten top layer, allows the formation of a crystalline bi-layer, albeit one with a high concentration of local defects as seen in Fig. 2.4. As the temperature approaches the bulk silicon melting point (1415 °C), the molten layer approaches the character of a regular melted material. The underlying substrate also can become less ordered due to an increase probability of adatom-vacancy formation and to a lowered step stiffness. As a result, the quenching from temperatures above 1300 °C will result in an amorphous-like layer covering a not so ordered crystalline substrate. After an RCA cleaning (which again should preferentially etch the more disordered top layer) revealed only a slight improvement in the step contrast showing that a kinetic roughening disordered also the underlying crystalline layer.

2.2.2 Atomic height islands on Si(001) surfaces

To reconcile the controversy related to the high temperature phase transitions observed on Si(001) surfaces is beyond the scope of this work. However, the morphologies we obtained on our annealed samples allow us to claim that a liquid-like state is present on the Si (001) surface at temperatures above 1150 °C. A similar debate is related to the (2×1) –> (1×1) phase transition on Ge(001). For more details see for example the paper published recently by Vroonhoven et al. [105] and references therein.

Figure 2.6 is a typical image of the vicinal Si(001) surface comprised of alternate straight and rough steps. The straight steps are called S_A and the dimers on the top terrace side of these steps are oriented perpendicular to the step edge. The

dimers align in dimers rows that are parallel to the S_A type of steps. The rough steps are called S_B and the dimerization direction on the upper terrace is parallel to the step edge. Theoretical predictions [106] and experimental results [84, 86] showed that S_B steps have a higher formation energy than the S_A steps. As a result the S_B step edges are much more jagged, often having a zigzagged shape. The unequal wide terraces form due to the anisotropy of the addimers diffusion constant (fastest along the dimer rows) [107-113] and also probably to a higher detachment rate from the high energy S_B steps.

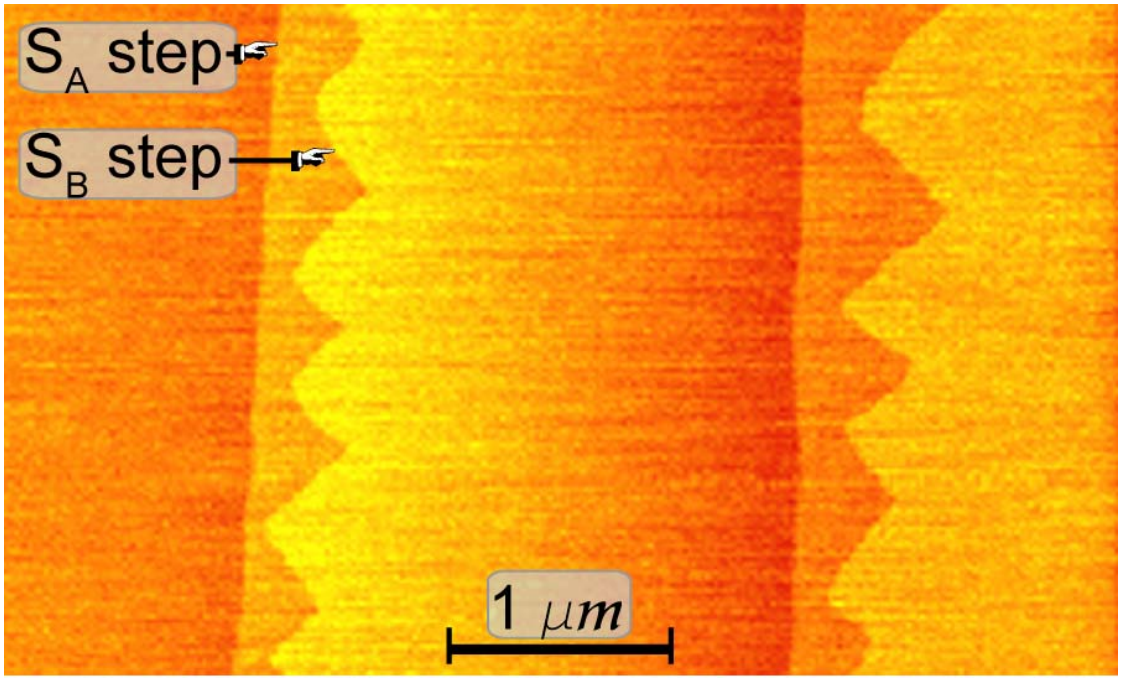

Figure 2.7. S_A (smooth) and S_B steps (jagged) on a Si(001) surface

The effect of step energy anisotropy caused by the different orientation of dimer rows can be seen in the Figs. 2.8 and 2.9. In both cases these structures were observed on samples that were flashed to 1300 °C, annealed at 1150 °C for several hours and then cooled down rather slowly (~ 2 °C/s). Fig. 2.8 shows the shape of several (2×1) reconstructed island that formed on top of (1×2) reconstructed terraces.

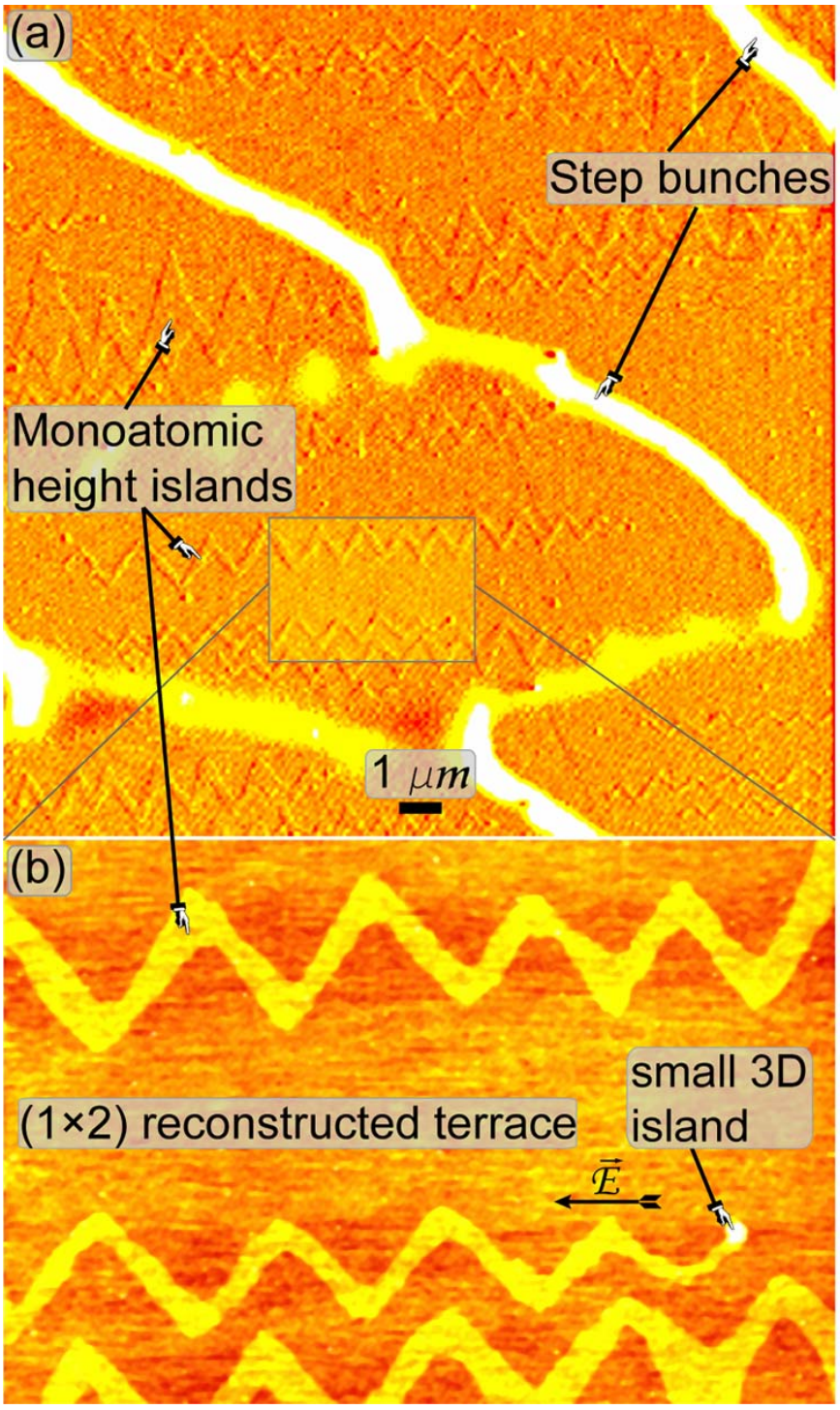

Figure 2.8. (a). 2×1 islands running almost horizontally on the wide 1×2 reconstructed flat terraces that span between step bunches. The long and thin islands are bounded by S_B steps. Some of the islands run from one step bunch to another, while others are pinned to some islands on the terrace. (b) Detail of the zigzagged steps seen in Fig. 2.8(a).

Due to the fact that these monoatomic islands are delimited by the S_B steps, they have this zigzag shape. This ondulated step structure on Si(001) is known to reduce the surface stress induced by dimerization [114, 115]. It is interesting to notice that if the distance between the islands is small, the island ondulation is in phase, while if the distance is large the ondulation is out-of-phase (but not necessarily in anti-phase). Now if the sides of the monoatomic height islands are S_A steps, then the islands will remain relatively straight, as seen in the Fig. 2.9.

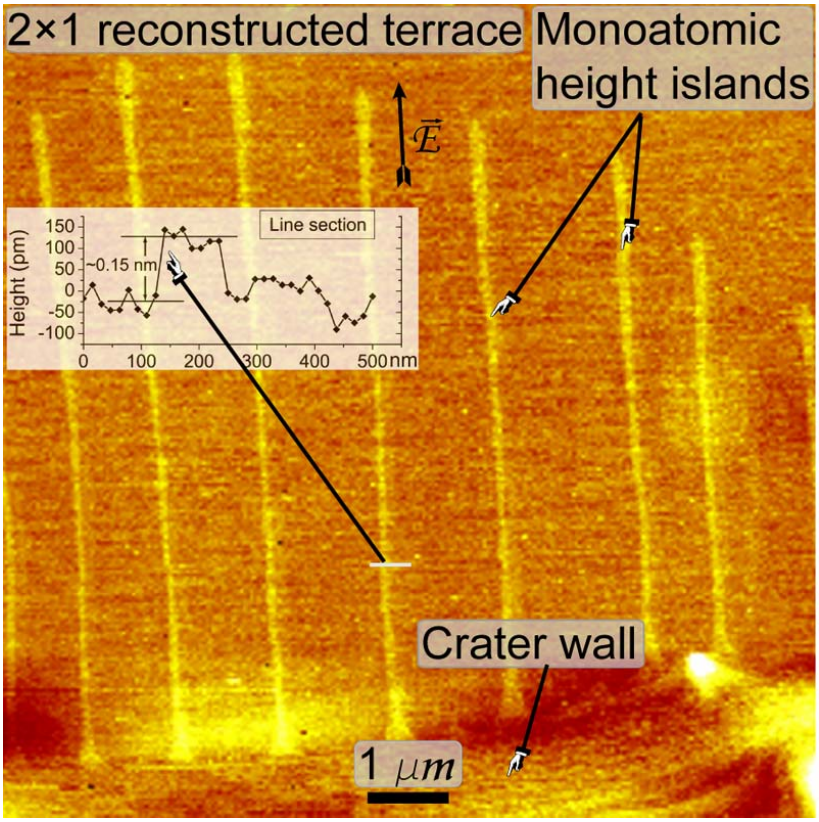

Figure 2.9. AFM image (rotated 90 ° to obtain a better image) taken from a different region of the same sample shown in Fig. 2.8. Straight islands bordered by S_A steps extending from a step-bunch that formed near the wall of an incomplete flattened bottom of a crater. A line section reveals that the islands are one interplanar distance in height (inset).

The fact that long, narrow, monoatomic height islands are present on the Si(001) surface after hours of annealing at temperatures where the sublimation is still a very important effect, makes us to believe that a liquid-like state can exist on the surface at temperatures below roughening transition. The surface is very smooth, with only a few small three dimensional (3D) islands, showing that the roughening transition was probably reached during flashing, but for sure not during annealing. Obviously the surface suffered some structural changes during the slow cooling down, but any annealing at lower temperature would only tend to smoothened out these surface features (thus especially removing or shrinking the features with a high surface area) as atoms detachment from the step edges is still an effective driving force even at temperatures as low as 1000 °C. During the relatively slow cooling procedure the elongated protrusions crystallize and reorganize in such a way that the local surface free energy (including the component of the elastic stress) is minimized. As we explained in the previous section, the survival of these islands (we referred to these as "protrusions"), even during a slow cooling procedure, requires large step free areas and a direct attachment to regions with high index plane (step bunches, 3D islands, crater walls), which function as a continuous source of adatoms as long as the temperature is above 800 °C. Again, the fact that the islands were elongated in the direction of the electric field confirms that the electromigration helped these islands to survive during the cooling procedure.

The sequence of events that we support for the Si (001) surface transition at around 1150 °C (partial dimer breakup causing surface melting and at higher temperature the surface roughens) agrees with the model suggested by Vroonhoven et al. for the high temperature phase transition on Ge(001). According to the authors [105, 116], LEEM and LEED studies showed that dimer break-up drives a reversible phase transition in the temperature range of 680 – 860 °C (with some dimer break-up

starting even at 630 °C). At temperatures above 860 °C, where the concentration of dissociated dimers reaches 99 %, a “non-reversible” surface roughening was observed. Normalizing these results to the melting temperature of silicon, the corresponding values for the reversible surface transition would be ~ 1050 °C, while the irreversible roughening transition should be expected at around 1300 °C. As the authored pointed out, the main difference in the behavior of the Si and Ge surfaces at high temperature resides in a three order of magnitude lower vapor pressure at melting point in the case of Ge (relative to Si). As a consequence, the kinetic effects due to the sublimation can be neglected for Ge, but in the case of silicon could result in a shift of the onset of surface melting toward higher temperatures. Above 1150 °C the Si(001) surface also starts to roughen (see also [109, 112]), but due to the smoothening effect of surface melting (and to a certain extent to kinetics effects), this roughening does not translate into a macroscopically irreversible divergence of height correlation function until the temperature goes above 1300 °C. We would like to emphasize once more that the structures formed during this phase transition can only be seen at room temperature if sinks for migrating atoms are not readily available.

We should notice however that our results are not a direct evidence of the surface melting. It is also possible that the structures described on this section could form due to the solid state diffusion along the step edge. The development of such elongated, monoatomic height islands on large, atomically flat terraces is favored by the reduction in the strain energy caused by surface reconstruction as described above.

2.3 Surface structures on Si(111) associated with (1×1) → (7×7) transition

2.3.1 Short review of the (1×1) ↔ (7×7) phase transition on Si(111)

The low temperature (7×7) reconstruction of the Si(111) surface was first described by Takanayagi et al. within the dimer-adatom-stacking fault model [117]. The reversible transition from a reconstructed to a disordered (1×1) surface phase was studied employing different experimental techniques (see for example the section related to this transition in Ref. [118] and references therein). The main conclusions can be summarized as follows. The (1×1)↔(7×7) is a first order phase transition that take place around 850 °C. It is characterized by an appreciable hysteresis over a range of up to 50 °C (depending on the rate of temperature change and the step density [119]) in which both phases coexists. In fact Kulakov et al. [120] observed that for samples cooled very quickly (1000 °C/s), the onset of the 7×7 LEED pattern is delayed down to 750 °C. Even faster quenched samples [121] do not contain any (7×7) domains on their surfaces at room temperature. Upon quenching many metastable reconstructions can form along with the stable (7×7) domains and disordered (1x1) regions [121-125].

The shape of the (7×7) domains is triangular and their edges orient towards $<1\bar{1}\bar{2}>$ type of direction [126]. Upon heating the (7×7) structures could also persist in a metastable state above the phase transition temperature due to the stabilizing effect of the elastic surface relaxation [87, 88, 127]. Even at ~865 °C, (at which the adatoms surface diffusion rate is relatively high) the decay rate of the (7×7) domains is of the order of tens of seconds and it seems to be limited by the rate of adatoms-vacancy creation [88, 128] or by the rate of formation-annihilation of the stacking-fault half unit [121].

Although not very important, the heating by direct current (DC) does affect the size of the (7×7) domains by biasing the diffusion of adatoms [129]. Computer simulations of the (1×1)↔(7×7) are limited to Monte Carlo variants [130] as molecular dynamics simulation are prohibited by the big size of the DAS structure and by the slow transformation rate.

2.3.2 Observed structures on step-free surfaces

Different types of surface structures are obtained if we cool down slower the Si(111) samples after annealing them below T_{sm}. Partial results related to this topic were published previously [131]. The results presented in this section were obtained using relatively lightly boron doped Si(111) (~ 0.8 Ω-cm) with 0.5 ° miscut angle.

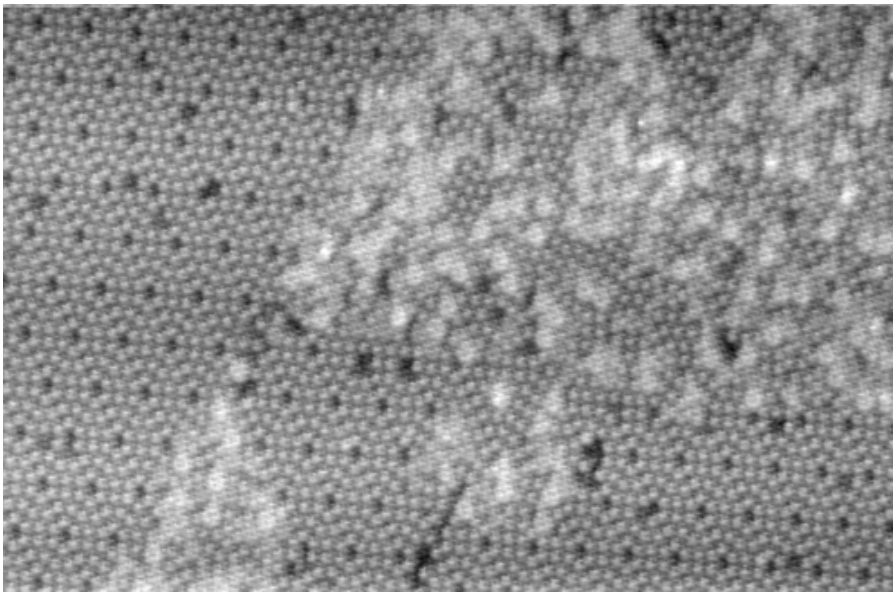

Figure 2.10. STM image of the Si(111) surface after quenching showing regular (7×7) reconstructed domains and disordered "clouds" of adatoms at the boundaries of (7×7) regions [132].

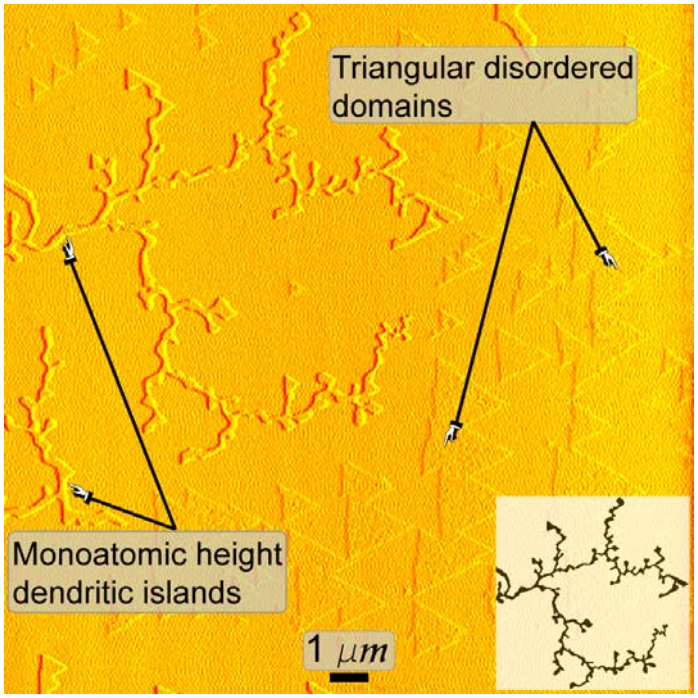

Figure 2.11. AFM amplitude image showing dendritic island structures (one bi-layer, ~0.3 nm, in height) and triangular disordered domains on the bottom of a 25×25 um crater. In the bottom right insert: the black and white (B&W) image of the island on the left that was used to compute the fractal dimension.

The triangular domains appear because of the transition from the (1x1) to the (7×7) reconstructed surface that take place at around 850 °C. Yang and Williams [122] showed that the disordered (1×1) surface phase density is about 6% higher than that of the low temperature phase (7×7). During the phase transition from (1×1) to (7×7), the excess atoms are expelled outside of the growing triangular (7×7) domains. On a normal, stepped surface, these excess adatoms are collected at the steps. But when the surface has very few defects or atomic steps that can accommodate the surplus of adatoms (which is the case with the atomically flat surfaces at the bottom of the craters), or when the cooling rate is very fast so that the adatoms cannot diffuse far enough to reach the sinks, the adatoms cluster in-between the growing (7×7) domains as triangular features, approximately 1.5 Å in height. In STM images [122, 132, 133]

these triangular features appear as somewhat disordered low density "clouds" of adatoms (Fig. 2.10) on top of the ordered (7×7) regions (or other metastable reconstructions able to accommodate a higher concentration of adatoms).

In Fig. 2.11 we observe at the bottom of the craters some bi-layer high islands with a dendritic morphology. Around these islands many triangular structures are also visible. It is worth noticing that close to the bi-layer high islands there are no triangular features, suggesting that the excess adatoms generated near the islands have been incorporated into the islands during their growth. This sample was annealed for 11 hours at 1150 °C. After that, the sample was cooled down to 550 °C in 5 minutes (2 °C/s) and then was quenched to room temperature.

The explanation of the origin of the dendritic islands, which extend from side-walls bounding the craters (in this case, due to the lower current density, the electromigration does not seem to be an important effect) requires two main ingredients: the protrusions that function as seeds and a rather high density of adatoms being released after the (1×1) → (7×7) reconstruction. At the annealing temperatures we used (1150 °C – below Si (111) surface melting transition, but close to it), the regions of the surface at the base of the side-walls bounding the craters will be ones with high-step density and consequently may disorder as described in the above sections. This process will generate liquid-like structures, to expand from the lower edges of the crater's walls towards the step-free region from the bottom of the crater even at temperatures slightly below the onset of surface melting. Upon cooling, some of these protrusions (most likely the biggest ones) will be "quenched-in" and persists at lower temperatures because of limited atomic mobility at temperatures below 900 °C. The protrusions can then act as sinks for adatoms generated by the transition from the (1×1) to (7×7) structure. Because of limited mobility, the morphology of the new islands resulting from adatom condensation will be of highly non-equilibrium and

driven by the local adatoms kinetics. The electromigration plays only a limited role in this case: while many protrusions are indeed parallel to the direction of current flow, other exists in different direction, and can potentially seed the development of other dendritic structures.

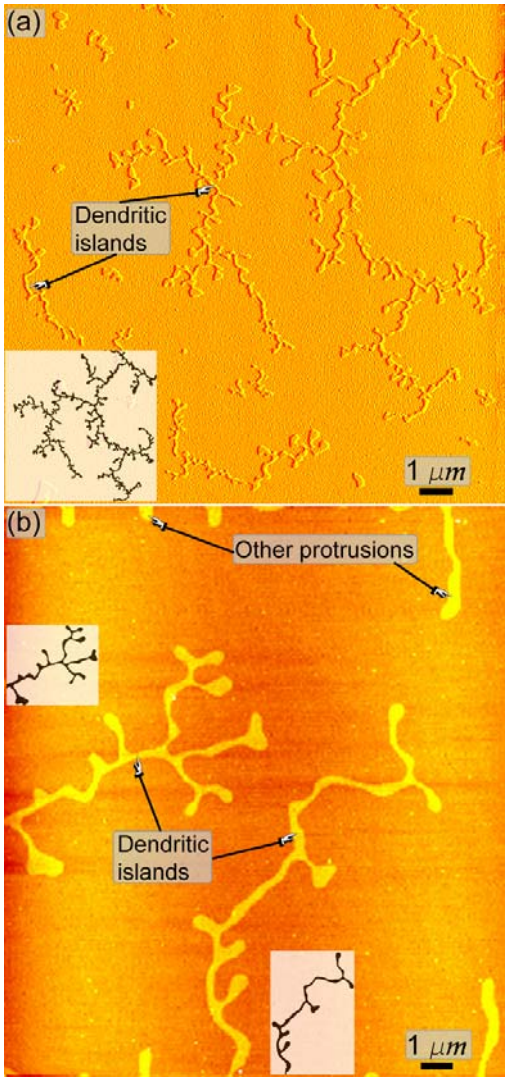

Figure 2.12. (a) Big dendritic island and many smaller dendritic structures are formed at a slightly reduced cooling rate. Somewhat surprising, the big dendritic island has almost the same fractal dimension like the island from Fig. 2.11. (b) A rather short annealing below the temperature of (1×1) → (7×7) transition results in less branched dendritic islands; left insert: the B&W copy of the horizontal (h) island, bottom insert: the B&W copy of the vertical island (v). Other protrusions can be seen running from the top and bottom walls.

The only difference in the thermal history of the samples on which the structures seen in the Fig. 2.12 with respect to that one from Fig. 2.11 is that a slightly slower cooling was performed (~1.8 °C/s), which allow some islands to nucleate inside the step-free region. In addition, in the case presented in Fig. 2.12 (b), the sample was annealed for 30 min at 800 °C resulting in a less complex structure. Nevertheless 800 °C is too low a temperature to effectively and completely remove these islands within this time-frame but a certain degree of smoothing did occur. As we highlighted across this paper, the main reason why we obtained such big and complex structures is that no steps or other extended surface defects are present at the bottom of our craters so that the excess adatoms cannot find readily available sinks as it is the case with vicinal stepped surfaces.

Small dendritic islands that resulted after (1×1) → (7×7) phase transition can be seen in Fig. 1(b) of Ref. [122] (where the samples were annealed at 600 °C following quench), or in Fig. 2(c) of Ref. [134] (where protrusions were observed on steps separated by large terraces after quenching).

Because for practical purposes we often need atomically flat surfaces (one application we described in a previous publication was to reduce the leakage current for the MOS capacitors built on atomically flat Si(111) surfaces [131]), we devised a two-step procedure to remove these "defects" from the bottom of the craters. First we cooled the sample very slowly (10 – 20 °C/hour) in the 1150 °C − 1000 °C range and then performed another extensive anneal (several hours) at 1000 °C. The idea is to keep the surface of the samples at a temperature below that of surface melting, but high enough to permit the protrusions to retract towards the crater walls by sublimation. If the model suggested in the previous paragraph is valid, a second long anneal around 800 °C should allow the excess adatoms generated by the (1x1) to (7x7) transition to reach the crater side-walls. After another several hours of anneal at 800

°C and a slow cooling to room temperature, we indeed obtained step-free surfaces at the bottom of the craters, with neither dendritic islands nor triangular features. Even more, in order to prove that high temperature anneal (close to the Si(111) surface melting temperature) is the cause for the appearance of protrusions, we performed this procedure to remove both the dendritic islands and the triangular domains and then we re-annealed a sample (without removing it from the UHV chamber) at ~1000 °C and afterward we quenched it. The resulting surface (Fig. 2.13) does not contain any protrusions but only (7×7) triangular domains. This time, due to the fast cooling, more than half of the surface is covered with regions that did not have time to (7×7) reconstruct and remained disordered.

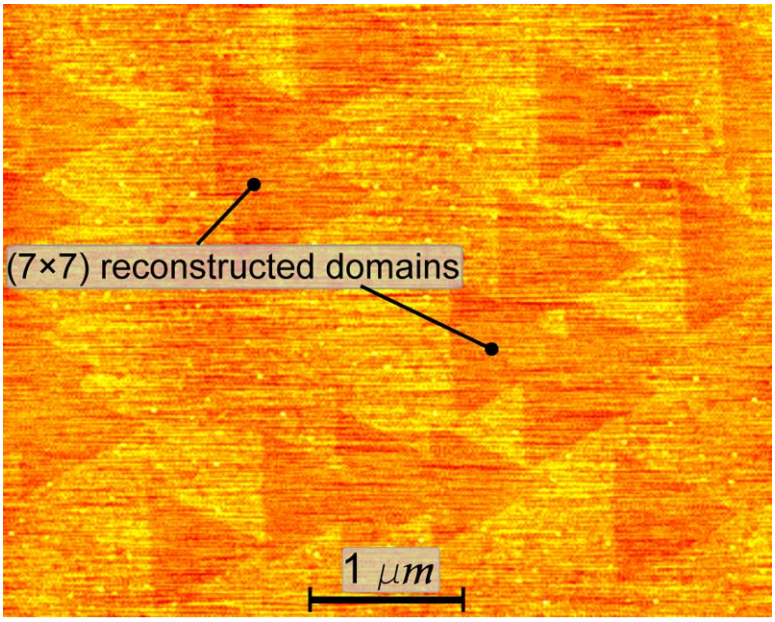

Figure 2.13. A fast quench from 900 °C in the absence of seed protrusions leaves most of the adatoms frozen at in the regions between (7×7) reconstructed domains (the triangular darker regions).

2.3.3 Fractal analysis of the observed dendritic structures

The mechanism described above for the growth of the dendritic islands is specific to diffusion limited aggregation (DLA) [135]. This model predicts the formation of 2D dendritic islands with a fractal dimension of ~1.7. Whereas many theoretical fractals obtained by modeling the fractal growth are only one lattice wide (and are using square elements), in the case of the surfaces with triangular symmetry (such is the case of Si(111) surface), the temperature range for fractal growth in DLA model is predicted to be much wider than on a square lattice [136]. More details about the fractal characteristics of DLA can be found for example in Ref. [137]. We have to keep in mind that even though the characteristics of mathematical models (such as DLA) can be described using the fractal theories, in nature all the structures can only be an approximation of ideal fractals, especially because these real objects do not show details and self-similarity on arbitrarily small scales. Therefore when we utilize a fractal mathematical model we have to be sure that the approximations used still allow for a correct description (see for example [138] or the debate related to the fractal analysis of Pollock's painting [139]).

Strictly speaking, the Hausdorff dimension is a better measure of a fractal (see for example [140], pp. 27-37), but this dimension is defined in practically any book about fractals). However its range of applicability in analyzing real images is relatively limited. The most often used technique to compute the fractal dimension of an object is the box counting method, which consists in breaking the image into boxes (squares in 2D) of a certain size and then counting the boxes that intersect the contour of our object. For a series of box sizes, the slope of the logarithmic plot number of boxes intersecting the contour versus 1/(block size) gives the box fractal dimension (D_B) of the analyzed object (a more exact treatment of the box dimension can be found

in [140], pp. 39-57 or in [137], pp.71-86). In other words, the box counting method measures the ratio of increasing detail with increasing scale, which corresponds with what a fractal dimension is.

In order to obtain the fractal dimension of the dendritic islands resulted after different heating regimes, we used the ImageJ [141] software v. 1.36 in conjunction with FracLac plugin v. 2.4d written by Karperien [142]. Although the calculation of the box counting dimension is relatively easy to implement in practice, it has its drawback in term of accuracy. For example the box counting methods often underestimate the real fractal dimension [143]. Used on linear fractals (Koch boxes), the box fractal dimension can be obtained even using only two boxes. Unfortunately all the real objects are nonlinear fractals and choosing the right set of boxes can be tricky [144]. The simplest way to generate a set of boxes is to use a linear series (with an increment of 1). The problem with this linear set of boxes is that in certain box ranges horizontal intervals could appear and this would reduce the measured fractal dimension. Therefore the meaning of the smoothed fractal dimension is that these regions where there is no significant change in the number of boxes that intersect our fractal are eliminated. One of the equivalent definitions of the box counting fractal dimension requires that the smallest number of arbitrary boxes should be used to cover the fractal ([140], p. 43). Of course a linear set of boxes does not meet this constraint, but even in this case one can find a way to efficiently cover the fractal so that only the minimum number of boxes (of a certain size) is used. The returned value is called minimum cover (eventually smoothed) D_B. Another way of generating the box series is to use only the factors of the size of the whole image. In this way a better coverage is expected. The name used in the FracLac plugin for this type of series is “relative series” (see the FracLac manual [FracLac]). The box counting method is also known to be sensitive to the box placement relative to the analyzed feature as the number of

boxes required to cover an image depends on where a grid is laid. In order to remove this influence the FracLac plugin allows multiple runs with the grid placement being assigned randomly within a set area. When this option is used the program finds a "most efficient cover" fractal box dimension where the least number of boxes to cover the image is used from all the grid positions tried.

A related method that can be used to determine the fractal dimension is the sliding box method, in which a set of boxes of fixed size are shifted across the image [145] in a similar the fast Fourier transformation is applied to a signal bounded by a moving frame. This method returns a so called mass fractal dimension.

In 2D, a line or a simple curve such as a circle has a fractal dimension of 1, while a filled rectangle (irrespective to its orientation) or a disk should return a fractal dimension of 2. We used this kind of simple geometric figures to check what would be the best settings for the FracLac plugin. Our conclusion is that the relative box series returns a fractal dimension closer to the real value of the filled (nonfractal in this case) image.

Using different simple geometric shapes in the manner described above we developed the following method to asses the box counting dimension so that the effect of choosing a certain maximum box size is minimized. We changed the parameters (the maximum box size) and we picked the value (of the maximum box size) with the highest correlation coefficient for the box sizes in the range 25-50%). Then we performed and extensive scan (using 20 start positions) for this box size. If there are two results with the same (maximum) value of the correlation coefficient, we performed the same extensive scan to both and if even this procedure returned the same correlation coefficient (but different fractal dimensions) we chose the highest value of the fractal dimension. For this value of the maximum box size we used the sliding box algorithm to obtain the mass fractal dimension.

The AFMs were rescaled so that all the analyzed images have about the same number of pixels per μm and then transformed into 8-bits gray-scale bitmap files. The number of pixels was increased with respect to the original AFM images in order to have a larger set of boxes available (see also [146]). Then we removed manually all the background. Finally we transformed our images in black and white pictures (see the inserts from Figs. 2.11, 2.12). In this way we eliminated any problems with the software not being able to follow properly the island edges, the issue that we encountered if overall software thresholding was used. Skeleton images (only the islands boundaries) are considered to return a better result in some cases [Foroutan99], but we consider that this introduce another artificial effect, as the thickness of the edge is only related to the image resolution. Even worse the scaling has a bigger impact on the result (as the thickness of the edge line covers more of the actual island thickness when a low magnification/resolution is used). On the other side less complex dendritic islands, but with thicker branches (as seen in the Fig. 2.12 (b)) will return a higher fractal values (as their shape approaches a filled simple geometric figure with a fractal dimension 2). So a bigger fractal dimension for a filled shape could mean a lower complexity if its thickness become important. For this reason we also included the fractal dimension for skeletal images.

The results for the fractal seen in the upper left part of Fig. 2.11 are presented in Fig. 2.14. The outcome of the box counting for the fractals from Figs. 2.11, 2.12 are summarized in the table 1. The values for the measured fractal dimension are below the 1.6-1.7 that would be expected for a dendritic structure that grew according to the DLA model. The main cause of these differences is of course the temperature that tends to reduce the complexity of the islands, therefore even relatively weak annealing effects reduce the fractal dimension. Theoretically, a DLA fractal should be only 1 atom thick, while in our case the islands have a thickness of about 50 nm.

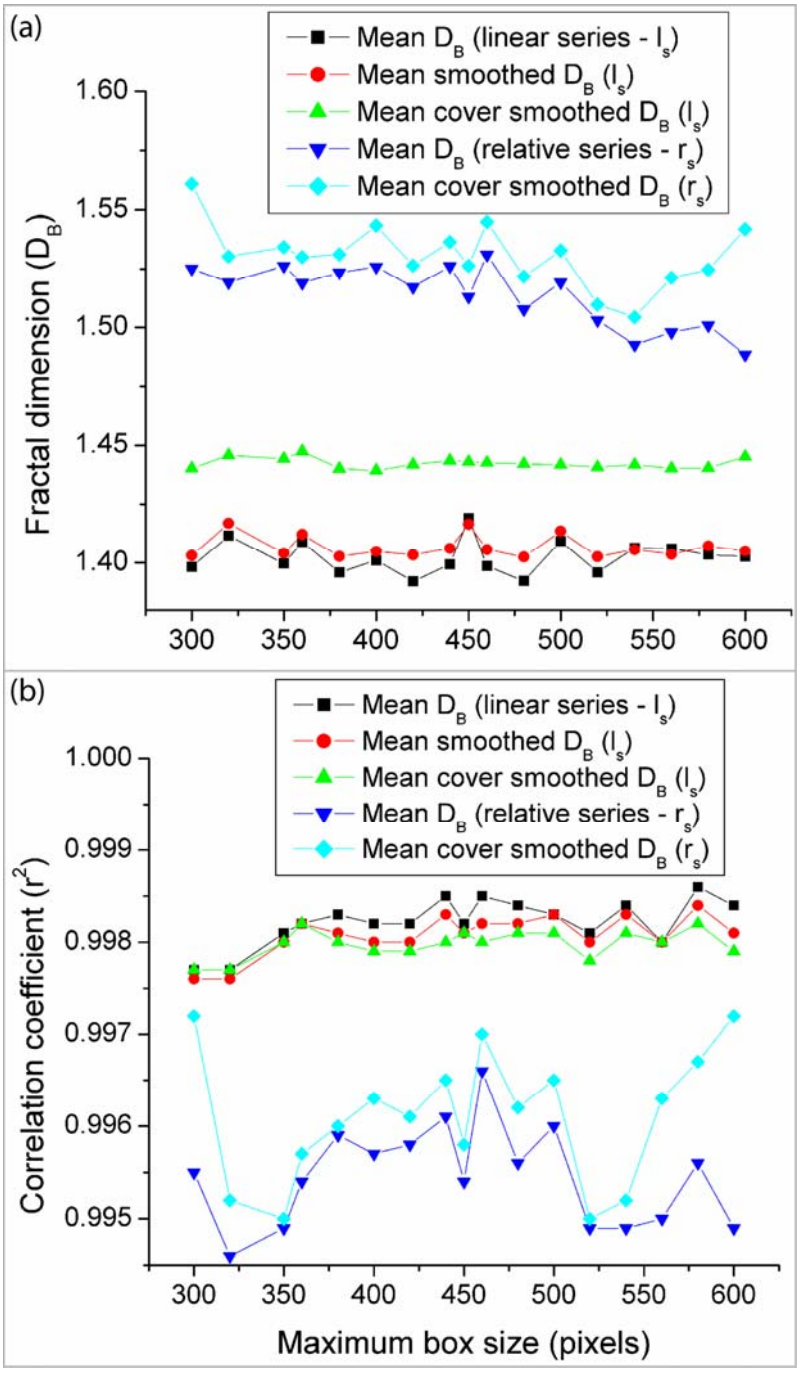

Figure 2.14. The variation of the box fractal dimension (a) and correlation coefficient (b) for the fractal island seen in Fig. 2.11, at different box sizes and for various calculations procedures.

Table 2.1. Summary of the results concerning box fractal dimension for the fractals included in the inserts of Figs. 2.11 - 2.12

	Circle	Fig. 2.11	Fig. 2.12 (a)	Fig. 2.12 (b) - (h)	Fig. 2.12 (b) - (v)
Image size	400×400	1200×1200	1250×1250	450×400	432×640
Expected fractal dimension	2 (1)	1.7	1.7	<1.7	<1.7
Box counting D	1.94	1.56	1.59	1.54	1.58
Sliding box D	1.98	1.56	1.63	1.53	1.54
Skeletal box D	1.08	1.39	1.47	1.37	1.35
Max # of boxes	120	300	625	150	108

2.4 Summary

New aspects of otherwise well known surface phase transition on silicon were revealed. By generating large step-free regions on the surface we succeeded to quench in surface structures that formed at high temperature without the need of very fast cooling rates. The main conclusions are following:

1. Si(111) surface melting takes place within a certain temperature range and starts from the step edges at about 1200 °C. At slightly higher temperatures these nuclei coalesce forming bands on the upper step terrace if the step density is low enough. We showed that these bands are composed in an amorphous-like atom clusters that are pilled up into a two bi-layer structure by the movement of the underlying crystalline step. Due to the absence of extended defects, the surface melting transition is shifted (with 5 – 10 °C) to higher temperatures for the atomically flat regions. However, it starts at lower temperatures for the regions with high step density such as step-bunches or crater walls. Under the influence of electromigration the molten layer formed

at the boundaries of atomically flat regions extends into these step-free regions as elongated islands that can be over 10 μm long. These long protrusions do not disappear even upon a relatively slow quenching and can be observed at room temperature with the AFM as two bi-layer high islands. We have shown that only the layer in contact with the crystalline substrate becomes crystalline, while the top layer, being more amorphous-like is selectively etched away during the RCA procedure. Above 1220 °C the whole Si(111) surface melts. The AFM performed on these quenched regions reveal a relatively smooth and featureless surface. At temperature above 1300 °C the steps becomes blurry and we associated this to a kinetic roughening at the crystalline – cvasi-liquid interface.

2. On Si(001) the surface melting is delayed by the high energy required to break the dimer reconstruction and occur around 1150 °C. When a large percentage of dimers break, the surface seems to undergo roughening, but this does not progress further than a few atomic layers due to the existence of a molten layer. Long and narrow monoatomic height islands can be seen on the surfaces cooled from 1150 °C. The shape of these islands depends on the type of steps that border its longer side: the (1×2) reconstructed islands are straight and parallel, while the (2×1) reconstructed islands are zigzagged and can be in-phase or out of phase depending on their relative distance. Creating elongated islands on atomically flat terraces, with island shape controlled by the step anisotropy and by elastic effects can potentially be a powerful tool for nano-patterning the surfaces.
3. On the Si(111) samples cooled with a rate of around 2 °C/s, the protrusions formed during surface melting acts as seeds for a dendritic growth of a bi-layer height islands in the atomically flat regions, during the (1×1) → (7×7) phase

transition. Using the box counting and sliding box methods we compared the fractal dimensions of the dendritic islands obtained as a result of (1×1) to (7×7) reconstruction with the result expected from the DLA model. From the fact that the obtained values of the fractal dimension is smaller that 1.7, we reasoned that the diffusion along the atomic steps is still important at temperatures as low as 800 °C.

Further experiments performed closer to thermodynamic equilibrium (using for example the setup deployed by Metois et al. [Metois00]) should check if our assumption that the main effect of the out-of-equilibrium sublimation consists in a shift of the onset of surface melting toward higher temperatures. We also consider that in the case of Si(001) the interplay of de-reconstruction, surface melting and surface roughening requires more theoretical and experimental studies.

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CHAPTER 3

EARLY MORPHOLOGICAL CHANGES ON SI(111) SURFACES DURING UHV PROCESSING

We present in this chapter two effects of interest in silicon surface processing. Firstly, we report on the evolution of surface roughness (starting from the regular, chemical polished wafers) under short UHV annealing. Secondly we show the effect of annealing on the detailed shape of pre-etched structures concentrating on the edges of the "walls" associated with craters (trenches) and mesas (ridges).

In order to investigate a continuous range of temperatures we intentionally clamped the samples tighter to their lower side so that a rather uniform temperature gradient is generated across the samples (Fig. 3.1(a) and (b)). The measured distribution of annealing temperatures on one of the samples is shown in Fig. 3.1(b). This sample had a temperature in the center area of around 1150 °C; it was annealed for 5 minutes and then quenched by turning off the power to produce an average cooling rate of about 120 °C/s in the 1150–700 °C range. At the annealing temperature, the temperature difference between the hottest and the coldest areas on the sample was about 100 °C as seen in Fig. 3.1(b). For comparison purposes, several other samples were uniformly heated using various annealing times (0.5-15 minutes) and temperatures (1000-1200 °C).

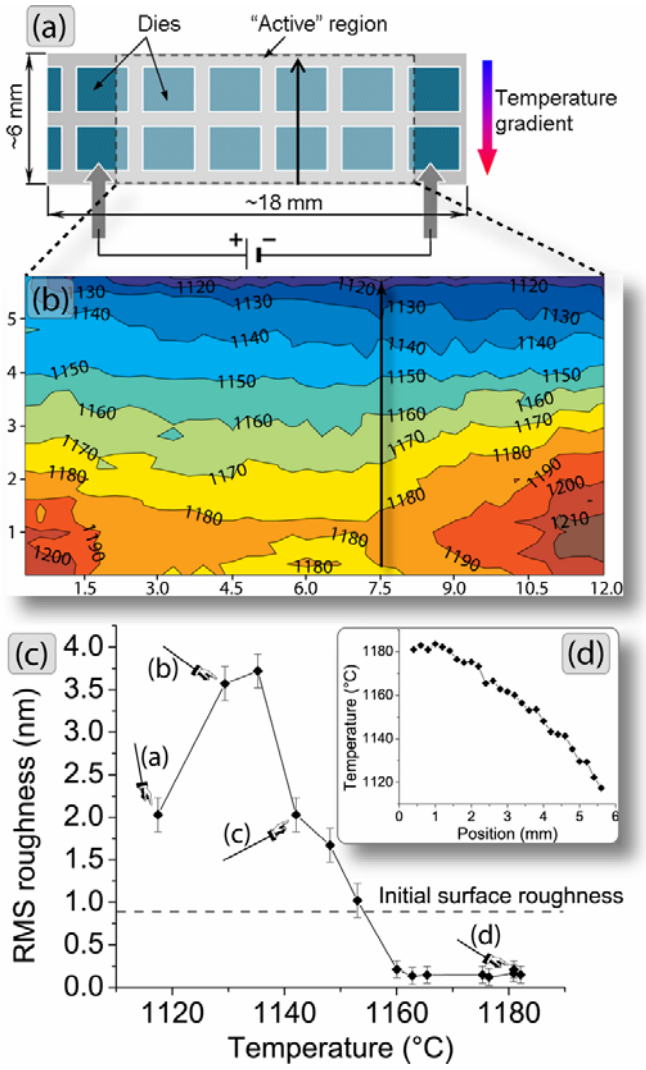

Figure 3.1. (a) Sample heating set-up; the dies contain arrays of craters and mesas of various sizes and shapes, but the roughness was measured along the vertical arrowed line, tens of microns away from any etched structure. (b) Contour plot of the sample surface temperature in the region between the rods of the sample holder ("active region"); the isothermal contours are marked in °C units; with the exception of the lower part of the sample, the temperature gradient is fairly one-dimensional. (c) Roughness variation across the sample as a function of annealing temperature; the letters represent the points corresponding to the AFM micrographs shown in Fig. 3.2; the error bars correspond to the average amplitude of the noise and is higher for rougher surfaces as different scanning parameters are needed in order to properly follow the surface features. (d) Temperature profile along the line where the roughness values were determined (see the vertical arrow in (a) and (b)).

3.1 Evolution of the surface roughness in the initial stages of UHV high temperature annealing

The root mean square (rms) roughness of the surface was measured after a 5 min anneal on unpatterned regions along the line shown in Figs. 3.1(a) and 3.1(b), where the temperature gradient was approximately constant. The value of the roughness was determined from 5×5 μm AFM scans, each scan being 0.4 mm apart. Before UHV annealing, the measured starting rms roughness of the surface was 0.88 nm. Using the temperature profile shown in Fig. 3.1(d) we determined the approximate temperatures in the scanned areas. In Fig. 3.1(c) we show the rms roughness from the cooler to the hotter edge of the sample. Representative AFM images and the corresponding height distribution histograms are shown in Fig. 3.2. Towards the lower edge of the sample, where the temperature was high enough, the surface reaches its thermodynamically stable structure of steps and flat terraces (Fig. 3.2(d)). Even though some small clusters form from adatoms during quenching, the height histogram is the narrowest in this case (Fig. 3.2(d')). On the upper side of the sample, where the temperature was lower, the terraces do not fully develop (Figs. 3.2(a) – 3.2(c)). The measured roughness becomes about four times *higher* than its starting value before decreasing in the higher temperature regions. Increased roughness of the surface can be qualitatively explained by the mechanism known in the thin film growth literature as Ostwald ripening. According to the Gibbs-Thompson relationship between chemical potential and local curvature, atoms from smaller and sharper wafer irregularities (higher curvature) will transfer to larger hillocks. As a result, smaller hillocks will shrink and disappear while larger hillocks will grow initially to produce the measured roughness maximum.

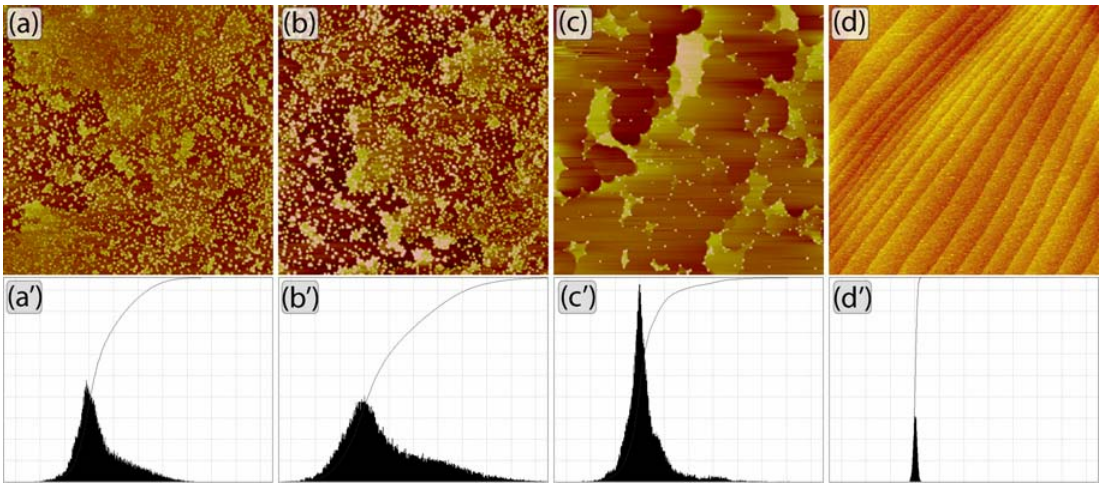

Figure 3.2. 5×5 μm AFM scans (performed in the positions marked by hand-shaped arrows in Fig. 1 (c)) and the corresponding histograms, showing the evolution of surface morphology after the same annealing time and increasing temperature. The vertical scale is 0-3 nm in (a) and 0-15 nm in (b), (c) and (d). For the histograms (a') – (d') the horizontal scale spans from -7 to 15 nm and the vertical scale (frequency) spans from 0 to 0.024. The origins of the horizontal axes correspond to the maxima of the histograms.

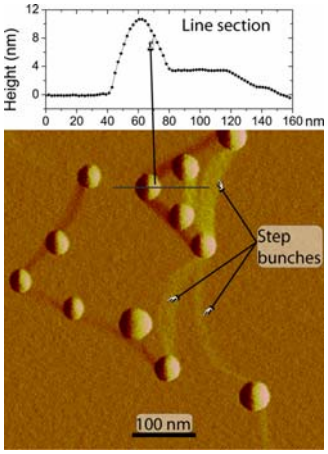

Figure 3.3. Detail of the spherical capped hillocks. Step bunches are created by the hillocks pinning the step flow. The inset at the upper side of the AFM image shows a line section across one of these hillocks.

At higher temperatures, even the largest hillocks shrink and flat terraces become easily visible (Figs. 3.2(c) and 3.3). From the line sections we can see that these large hillocks are approximately spherical caps with a rather wide size distribution as seen in the histograms. Most of them attain a height of 5-10 nm (Fig. 3.3). On the other hand, at the lowest temperature, many small islands exist on the surface instead of fewer larger ones (Fig. 3.2(a)) and, as a result, the measured roughness is smaller, but it is still higher than the initial roughness.

It is interesting to observe that the hillocks hinder the step movement, resulting in semicircular step arrays around each of them; such step distributions are also observed in the transition from active (etching) to passive (growth) oxidation regimes of the Si(111) surface [1]. To test if the hillocks could have formed due to surface segregation of oxygen which is known to be present in wafers grown by the CZ process [2] we subjected the sample to an HF dip, which should selectively remove the silicon oxide; no measurable change was observed in the size of these islands. Thin silicon oxide desorption in UHV is also known to roughen the underlying silicon surface [3-6], but since we removed the oxide and passivated the silicon surface by dipping the samples in HF shortly before loading them in the UHV chamber, we consider that this process is insignificant in our case. The time scale would also be different, as a 0.3 nm oxide film completely desorbs in about 2 minutes at 720 °C [4, 5], a temperature much lower than used in our experiments

A quick estimation of the hillocks decay rate using the time dependence characteristic for surface transport: $\Delta h = B \cdot t^{1/4}$ [7] with the prefactor B = 87 Å/s$^{1/4}$ (determined by extrapolating the data from the Ref. [8]) gives a decay time for a 20 nm isolated mound of about 30 seconds at 1100 °C. Including the initial ripening stage, we should be able to obtain a flat surface (albeit a stepped one) in a matter of minutes. In contrast, the time needed to remove by step flow all the atomic steps over

a surface of 35 μm at the same temperature (in a direction parallel to the step flow) is of the order of 1.5 hours for a 0.5° miscut (corresponding to an wedge of 1000 bi-layers in height) and using a sublimation rate of 0.2 bi-layers/s [9]). Therefore for obtaining an atomically flat surface still a rather long annealing (or higher temperature) is needed. However, in many applications where only flat but stepped surfaces are smooth enough the thermal budget could be substantially lowered.

3.2. Effect of annealing on the shape evolution of the pre-etched structures

In this section we present observations on the way the detailed surface shapes at the edges of mesas and craters develop during UHV annealing. This problem was addressed in two theoretical classic papers by Mullins who considered different possible transport processes [10, 11]. A striking feature of the solution for the developing profile of a mesa or crater edge due to surface or volume diffusion is its spatially oscillatory character. Experimental evidences were first related to the thermal grooving at grain boundaries (see for example [12]). However, this theory should only be valid for isotropic solids (e.g. glasses) but may also be applicable to crystals above their roughening or premelting transitions. Liu et al. observed that even in the one-dimensional case of the spreading of a step bunch relaxation (with terraces in-between much wider than the equilibrium step separation), the isotropic continuum model yields to the same scaling exponents as the discrete step model with local conservation [13].

High index silicon surfaces are known to disorder at temperatures much lower than those for low index planes such as Si(111) [14, 15], so that we might expect the predictions of the Mullins theory to apply to high index planes at very high

temperatures. This is indeed consistent with what we observe experimentally: the edge profile is evolving according to the prediction of continuum theory especially in the very early stages of annealing when the surface roughness is still relatively high.

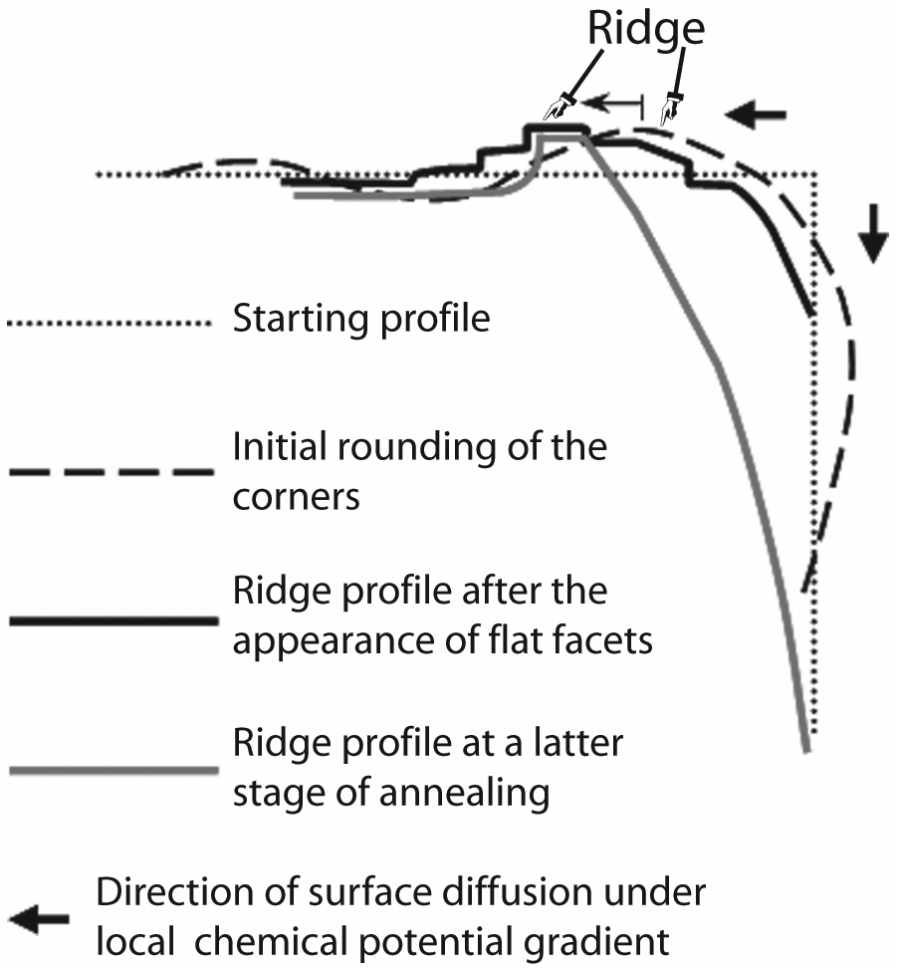

Figure 3.4. Schematic of the type of profile predicted by isotropic continuum theory (dashed line) vs. the ridge shape obtained (full lines). One can see that due to the outward step flow the ridge grows slightly away from the corner and flat facets forms. At a later stage of annealing the ridge narrows and, as the slope of the crater wall decreases, it occurs right at the edge (see also Figs. 3.5 and 3.6).

Figure 3.4 is a summary of the observed edge shape development, while Figs. 3.5-3.7 present some representative AFM images. As indicated in Fig. 3.4, the edges of mesas develop ridges in qualitative agreement with the Mullins' prediction but as the annealing progresses and the average roughness of the surface decreases the crystallographic nature of the substrate becomes evident through the appearance of facets on the profiles and well defined step arrays. Subsequently we have studied how these arrays of curved steps develop at the edges of both mesas and craters as annealing proceeds.

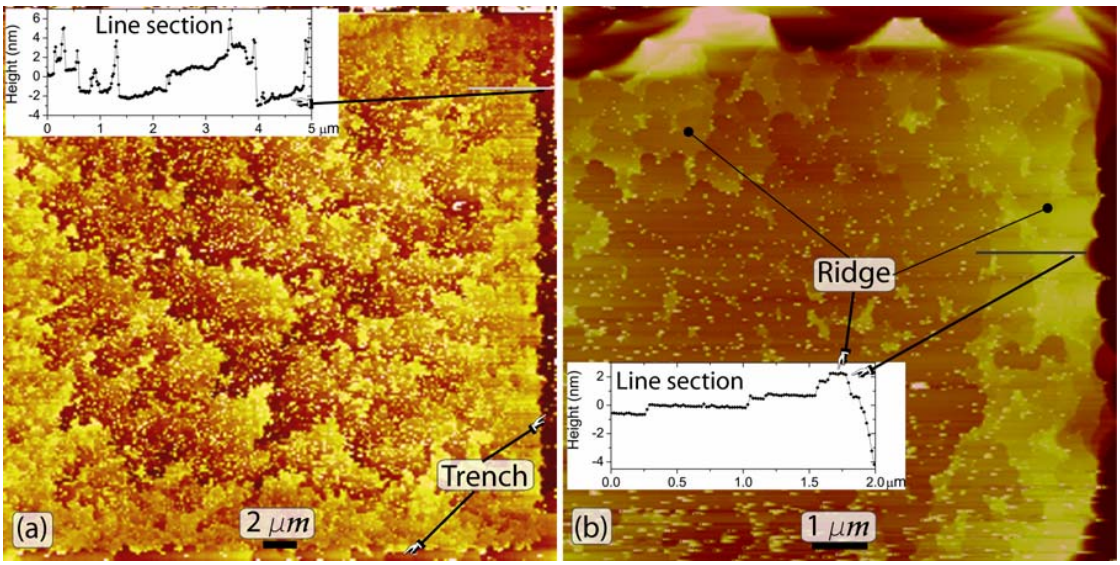

Figure 3.5. Initial stages of formation of (a) a trench at the border of a crater and of (b) a ridge at the upper edge of a mesa. The insets show sections across the trench and the ridge respectively.

Figures 3.5 (a) and (b) show that at an early stage of annealing neither the trenches nor ridges are well defined along the whole boundaries. Furthermore, due to the wafer miscut and to the flow of steps away from the lowest region of both kinds of structures, the trenches and the ridges will eventually disappear of break down near

the regions with lowest elevation as noted earlier by Chang and Blakely [9] (due to the wafer miscut, the lowest region is always near one edge of any kind of structure).

Although we had hoped to use the presence of ridges formation to create step free areas on the top of mesas [9], the ridge break down prevents this from happening (Figs. 3.6 and 3.7). However, as reported earlier [9], the presence of the ridge does allow the formation of regions with single atomic steps separated by wide atomically flat terraces (Fig. 3.7). It is interesting to notice that due to steps flowing from the edges towards the inner area of the mesas [16] the ridge starts to develop a little bit inside of the mesas (Fig. 6) and only later on it narrows and we can see it right at the edges (Fig. 3.7).

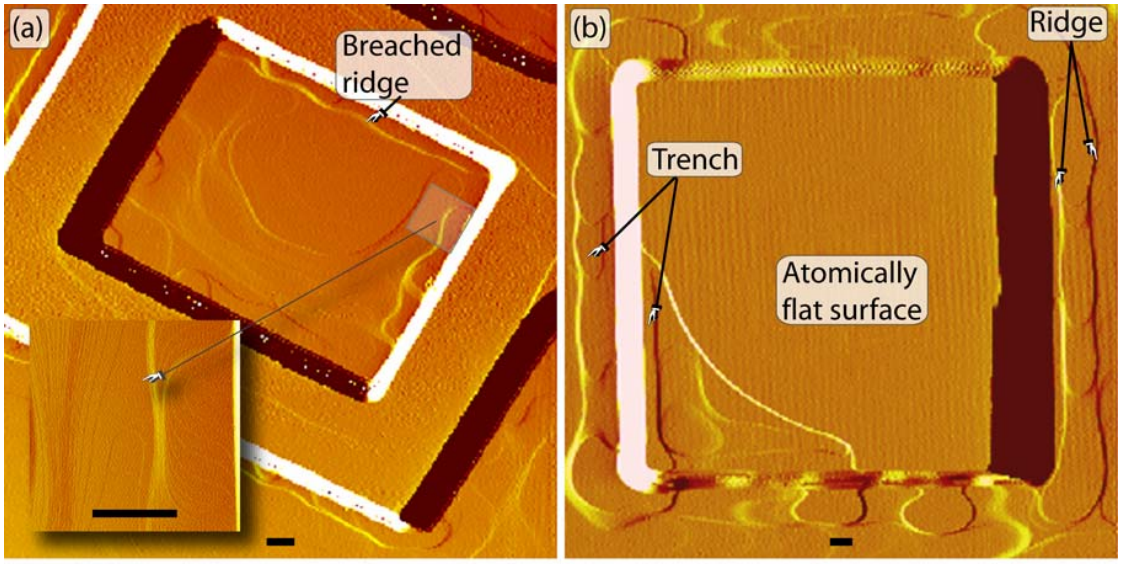

Figure 3.6. Mesa (a) and crater (b) showing ridges developing slightly away from the edges. The scale bars represent 2 μm. In (a) one side of the ridge almost completely disappeared; in the inset a detail of the ridge is shown. In (b) the step flow at the bottom of the crater created a large step free area. A trench is still visible in the lower left corner where the steps were not yet cleared.

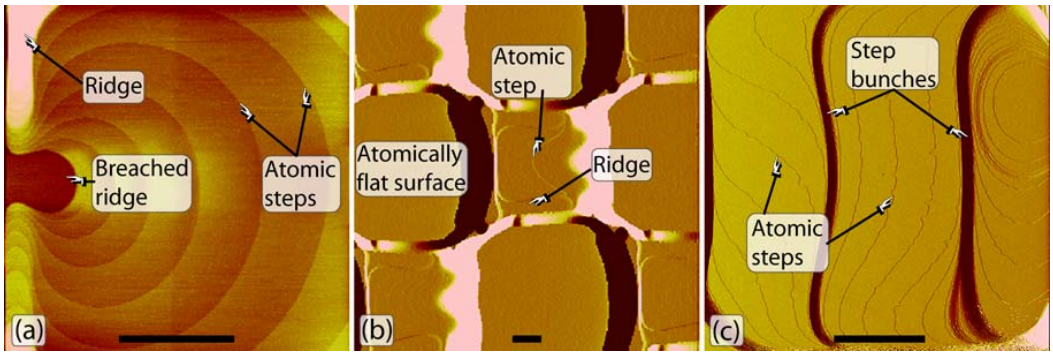

Figure 3.7. Three later stages of development of a ridge (increasing annealing time); (a) the ridge surrounds all four sides of the mesa with the exception of a small breached region; (b) ridges can be seen along three edges of mesas (the contour of the highlighted step was enhanced by hand); in (c) the ridge has practically disappeared. Widely spaced steps be seen in all of these AFM images. Scale bars = 5 μm.

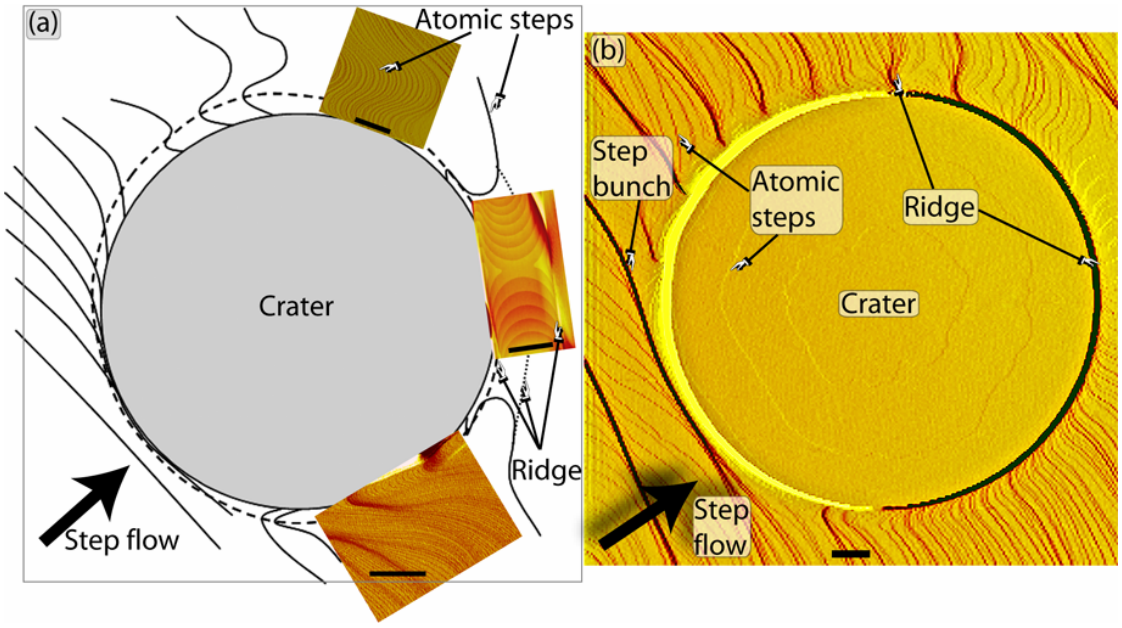

Figure 3.8. (a) Schematic of the process that maintains a ridge around a crater even after long annealing times; due to continuous step flow from the surrounding miscut area a steady state step distribution occurs as steps are kinetically pinned by the upper edge of the crater. The insets are AFM images showing typical step distribution at different positions around a crater. (b) Large AFM scan showing the steady state ridge at later annealing stages. The scale bar is 5 μm in all these AFM images.

The evolutions of trenches that form at the edges of craters (Fig. 3.5(a) and the lower left corner in Fig. 3.6(b)) is similar to that of the ridges on mesas. It should be noted that these trenches do *not* originate from the RIE micro-trenching that has been reported in other papers [17-23]; our AFM analysis showed that no detectable trenches existed before UHV annealing.

At a later stage of annealing, due to evaporation in the UHV system, both the ridges at the edges of mesas and trenches at the edges of craters eventually disappear (Fig. 3.7(c) and Fig. 3.8(b) respectively). As a result of steps flowing from the edges, the mesa's ridge disappear at first from the lowest side and in the end remains only as a step bunch in the uppermost side of the mesa (Fig. 3.7(a) – (c)).

The step distribution around an isolated crater on an otherwise unpatterned region is of interest for comparison with recent theoretical predictions [24]. On the top edge of the wall surrounding an *isolated* crater the evolution of the ridge is initially similar to that at mesa's edge – see Fig. 3.6(b)). However, at a later annealing stage, the unlimited continuous step flow across the surface due to evaporation can dynamically sustain most of the ridge surrounding an isolated crater. As shown in Fig. 3.8, incoming steps are annihilated by steps making up the crater wall, but the ridge is maintained around most of the perimeter. The steps thus acquire an asymmetric S shape near the crater being kinetically pinned in the high step density regions situated near the upper crater's edge. This is in qualitative agreement with the recent analytical model of Katifori and Nelson for steps interacting with a surface defect such as a scratch or an etched trench [24]. As seen in the Fig. 3.8 this type of step distribution is indeed observed in certain regions near the craters. On the other side of the crater (upper right side in Fig. 3.8), steps flowing around the crater from both sides create a very clear trough through band - antiband formation (using the terminology proposed by Latyshev et al. [25, 26]) and step annihilation.

3.3 Conclusions

We have examined the effect of annealing at high temperature for short periods (minutes) on the Si(111) surface morphology. Initially the surface roughness has a non-monotonic evolution with the maximum roughness being about four times its initial value. This temporary increase in the measured rms surface roughness is attributed to an Ostwald ripening process. Secondly, we have shown that the evolution of the shape near the initially sharp edges of etched structures, in the early stages of annealing, is consistent with the prediction of the continuum theory, resulting in the formation of trenches at the bottoms of craters and of ridges at the tops of mesas. However at later stages, flat facets occur separated by step bunches. Whereas the trenches at the bottom of crater arrays and ridges at the top of the mesa arrays shrink and eventually disappear, the ridge that forms around an isolated crater acquire a steady state profile and survives indefinitely.

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CHAPTER 4

APPLICATIONS OF THE ATOMICALLY ENGINEERED SUBSTRATES: (1) REDUCING LEAKAGE CURRENT IN MOS CAPACITORS (2) INDUCING TEXTURE IN POLYCRYSTALLINE PENTACENE THIN FILMS

In this chapter we will present the results related to two applications that we developed using our substrates processed by UHV high temperature annealing. First, we have built MOS capacitors on three types of Si(111) surfaces viz. atomically flat surfaces, normal (stepped) surfaces cleaned in UHV by high-temperature annealing, and normal, RCA cleaned wafer surfaces. The leakage current through the oxide was measured for all three cases. In another application, Si(111) substrates with regular arrays of atomic steps were used to induce azimuthal alignment of crystals in thin polycrystalline pentacene films. Pentacene films deposited on heated samples, at a low deposition rate, show significant azimuthal alignment of the pentacene crystals relative to the atomic steps.

4.1 MOS capacitors built on atomically flat surfaces

To investigate the influence of surface roughness we have built MOS capacitors (Fig. 4.1) on three types of silicon surfaces: atomically flat surfaces (A), stepped surfaces cleaned in UHV by high-temperature annealing (B), and normal (not annealed in UHV), wafer surfaces (C). The wafers were Si(111) B-doped, with a resitivity of around 0.8 Ω-cm.

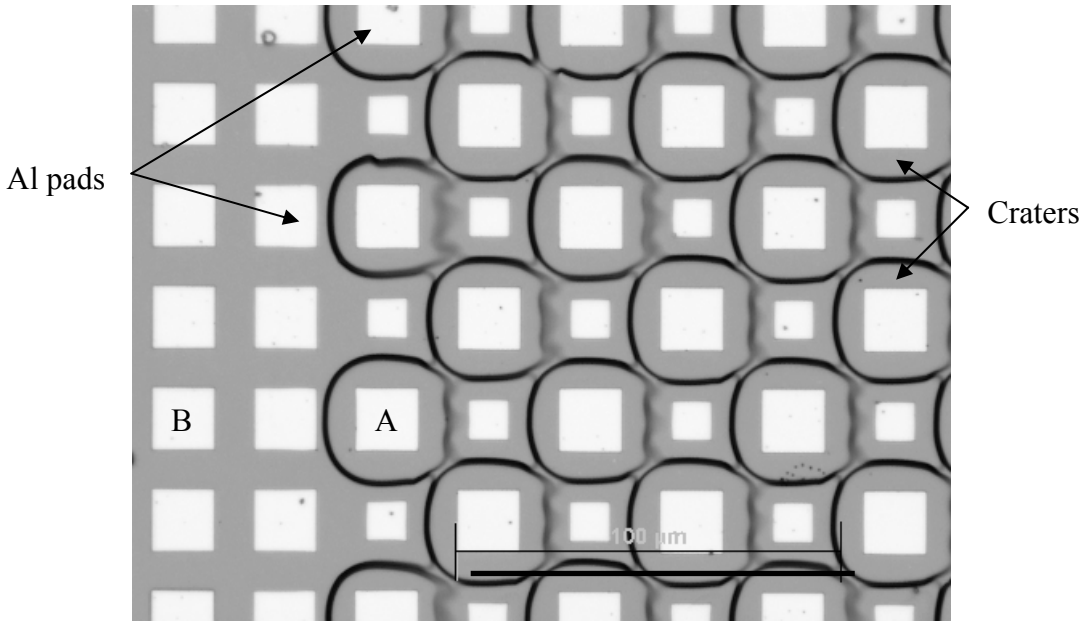

Figure 4.1. Optical microscope image of MOS capacitors built on (A) step free and (B) stepped Si(111) UHV annealed surfaces. The scale bar represents 100 µm.

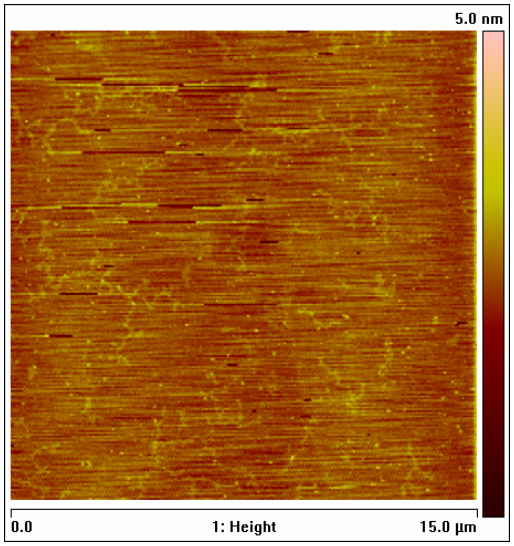

Figure 4.2. The topography of the oxide surface after growing 3.5 nm of oxide at 750 °C, revealed by AFM. This image is from the bottom surface of an etched crater. Although the oxidation doubles the roughness of the surface, one can still observe the dendritic islands replicated almost unmodified by the oxide layer (see also Figs. 2.11, 2.12 for the surface morphology before the oxide growth).

The summary of the procedure used to build the MOS capacitors is as following (see also Appendix A.2). After the UHV thermal treatment, the samples were RCA cleaned, dipped in 5% HF to obtain hydrogen terminated surfaces and then thoroughly rinsed with DI water. The oxidation was performed in a CMOC clean, atmospheric oxidation furnace, at the Cornell NanoScale Science and Technology Facility (CNF). Oxide layer between 3.5 and 12 nm were grown in O_2/N_2 gas mixture (10%O_2, 90%N_2 by volume) at temperatures ranging from 750 °C to 900 °C, followed by a 10 – 15 minutes anneal in nitrogen at process temperature. The thickness of the oxide layers was measured using a variable angle spectroscopic ellipsometer. If the oxidation temperature is below 800 °C, a significant roughening of the surface occurs (Fig. 4.2). While the rms roughness of the step-free surfaces was about 0.15 nm before oxidation, that of the oxide surface was around 0.3 nm. Since there is considerable evidence that the silicon oxide conforms to the underlying silicon surface, we believe that the Si/SiO_2 interface also becomes significantly rougher if the dry oxidation is performed at temperatures below 800 °C. While annealing the oxidized samples at higher temperatures is expected to smooth the oxide and the Si/SiO_2 interface [1], we were unable to keep the O_2 partial pressure sufficiently low to prevent additional oxidation.

After the oxidation, a forming gas anneal (N_2/H_2) was performed on samples with 3.5 nm oxide thick layers, at a temperature of ~ 450 °C for 30 minutes, with the purpose of reducing the interface traps density (see for example ref. [2]).

Subsequent to the hydrogen anneal, a 350 nm aluminum film was deposited over the whole surface of the samples utilizing e-beam evaporation. Using an image reversal technique for the second level of lithography, arrays of rectangular metal contact pads (18×18 micrometers) were created at the bottom of the craters, inside the step-free areas. Similar pads were also created on the surrounding unpatterned regions

that contain numerous atomic steps. The resulting pattern can be seen in Fig. 4.1. After etching off the oxide on the back side of the samples, a 250 nm layer of aluminum was deposited as a second electrical contact. All the above procedures were also performed on a reference, unpatterned wafer, which was RCA cleaned before oxidation but not annealed in UHV.

The leakage current was measured for these capacitors, tracing I-V characteristics and testing against the Fowler-Nordheim (FN) theory. For the oxide layer thicker than 3 nm, the direct tunneling current is negligible and the main component is due to the Fowler-Nordheim tunneling (Fig. 4.3). The slope of the FN plot is related to the effective thickness of the oxide. The rougher stepped surface was expected to show a higher tunneling current according to the model developed by Majkusiak and Strojwas [3].

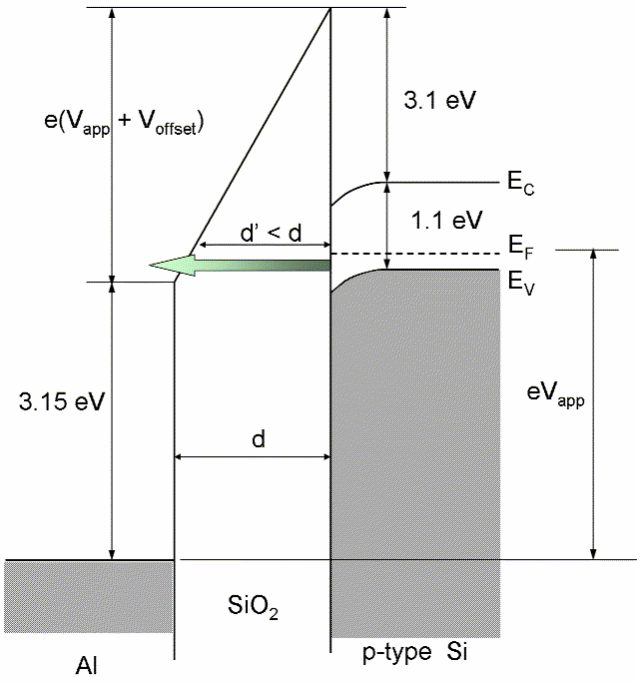

Figure 4.3. Energy band diagram for an Al – SiO_2 – Si structure under the bias conditions in which the Fowler-Nordheim tunneling occurs

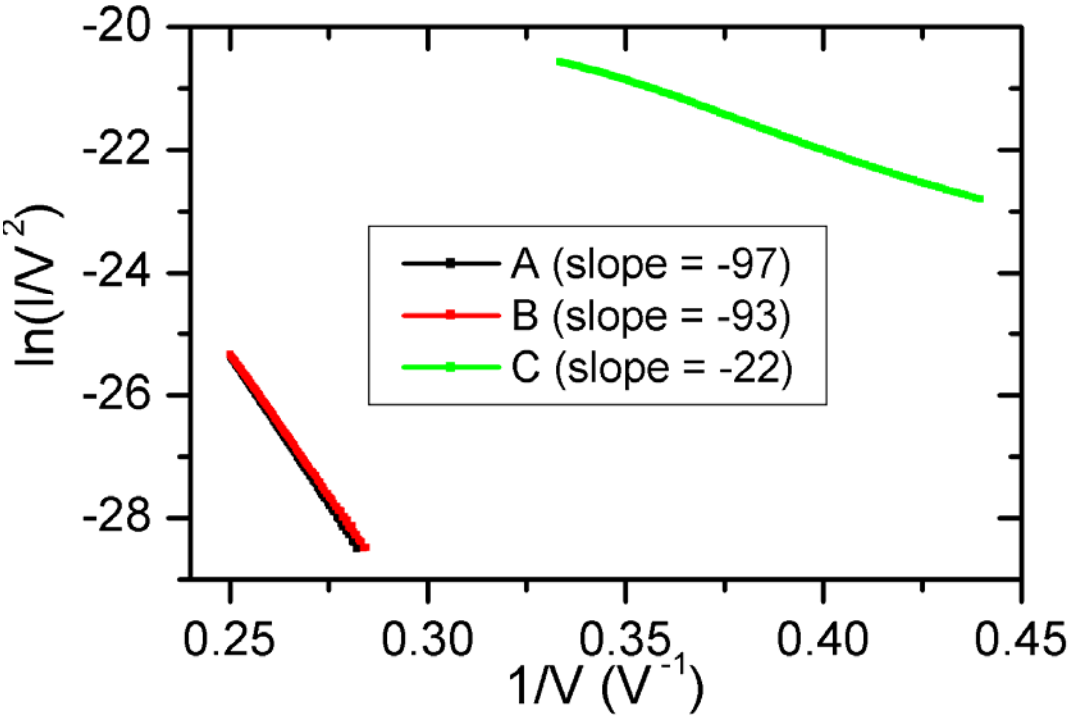

Figure 4.4. Fowler-Nordheim plots for an average of 5 capacitors built respectively on step-free surfaces (A), stepped surfaces (B) and normal, RCA cleaned Cz wafer surfaces (not annealed in UHV). The slopes of these plots can be interpreted on the basis of a simple model [3, 4] to be proportional to the effective thickness of the oxide tunneling barrier.

Initial results obtained in our group showed that, for an oxide thickness of about 5 nm, the ratio of the slope of the FN plots for the capacitors on areas outside the craters to the slope for the capacitors on step-free surfaces is about 0.9 [4]. Our more recent investigations also indicated that the slope of the FN plot is about 5% higher for capacitors built on step-free surfaces than on stepped surfaces for 6 nm oxide and about 10% higher for 5 nm oxide [5]. There is no measurable difference if the oxide is thicker than 8 nm. While it was expected that this difference should increase for thinner oxide, our results for 3.5 nm oxide thickness [6] showed only a

~5% higher slope for the capacitors built on step-free surfaces (Fig. 4.4). A possible explanation for this result is that the thinner oxide requires a lower growth temperature, which in turn is known to create a rougher Si/SiO_2 interface (see for example reference [7]).

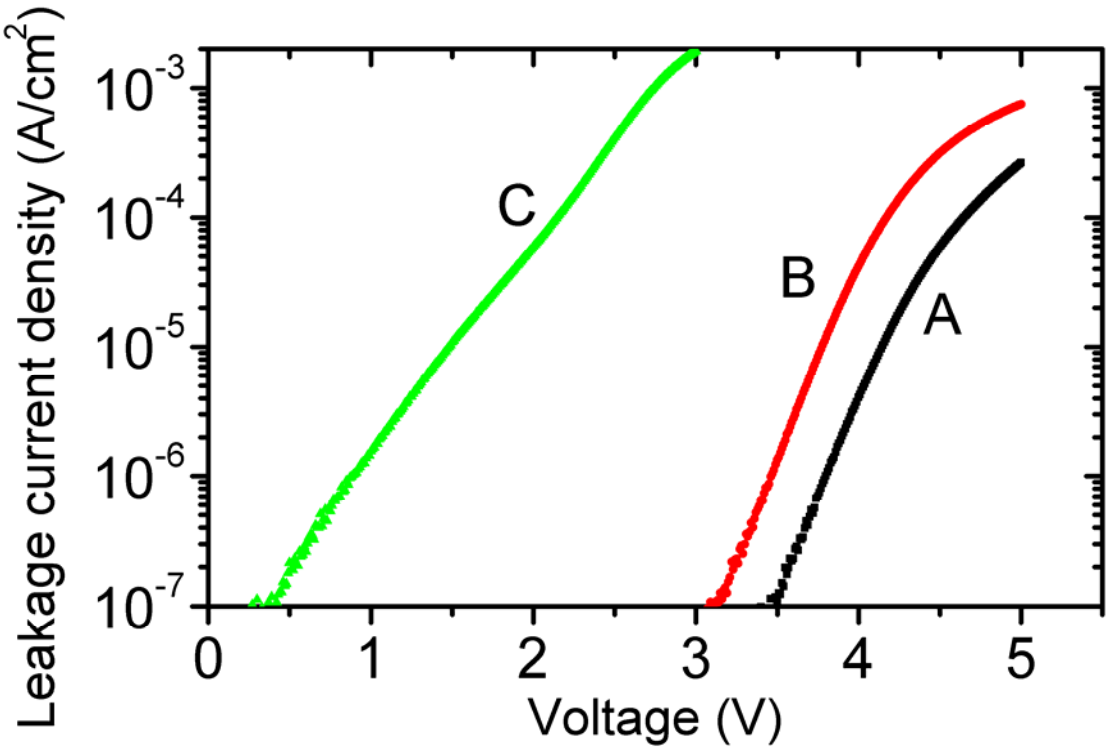

Figure 4.5. Average leakage current density (the same data shown in Fig. 4.4 as FN plots)

Nevertheless, for a given voltage, the tunneling current is lower for the capacitors built on step-free regions than for those on the UHV treated stepped surface (Fig. 4.5, characteristics (A) and (B) respectively). Even though the difference between A and B curve is relatively small and within the range of data scattering, a much higher leakage current was observed for capacitors built on (C) samples that were not UHV processed. In that case the slope of the FN plot is several times smaller

than for the sample cleaned in the UHV chamber by high temperature annealing (Fig. 4.5). Comparing the values of our leakage currents with those published in the literature [8], we can comment that the capacitors build on UHV processed samples shows a lower leakage current density , while those built on regular, RCA cleaned wafers are worse than previous published results (see Fig. 4.6).

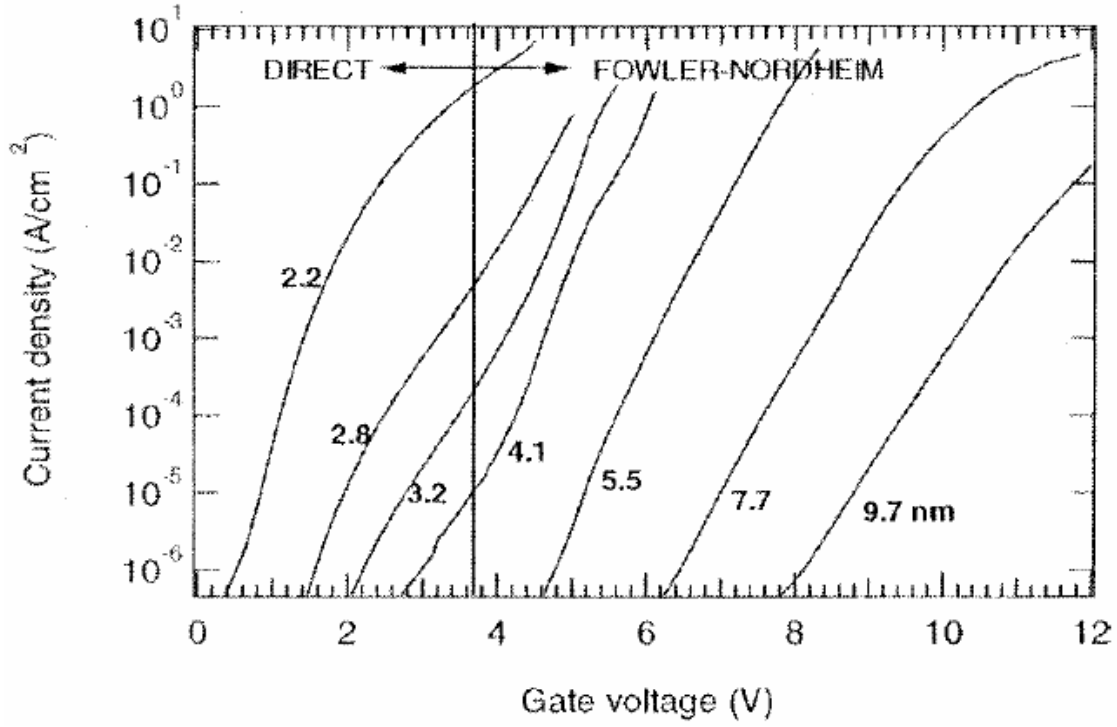

Figure 4.6. Leakage current densities for different oxide thicknesses as published in [8]. The figure was taken from [9] (Fig. 48, p. 2077).

The main conclusion of these experiments is that for an oxide layer thinner than 8 nm, the leakage current for capacitors built on stepped surfaces is higher than for capacitors built on step-free surfaces. The reason for this behavior could be the reduced effective thickness of the oxide near steps and an enhanced electric field at the

steps. The leakage current is however much smaller for the UHV annealed substrates than for capacitors on the wafer that was not cleaned by UHV annealing.

The ongoing experiments are oriented towards building capacitors with silicon oxide layers below 3 nm grown at temperature above 800 °C. Capacitance-voltage measurements will also provide a test for the existence of interface states.

4.2 Using atomic steps to induce texture in polycrystalline pentacene films

4.2.1 Introduction

Pentacene is an organic semiconductor being studied as candidate for cheap, large area organic based electronics [10-12]. While single-crystal field-effect transistors of pentacene show a charge carrier mobility of up to 2.3 $cm^2/(V \cdot s)$ [13], the mobility measured on polycrystalline thin film transistors is almost an order of magnitude smaller [14, 15]. One source of this reduced mobility in polycrystalline pentacene film is charge carrier scattering at the grain boundaries [16, 17]. In this section, we report that using atomic steps as preferential sites for nucleation, under proper growth conditions, we have achieved good azimuthal alignment of the pentacene crystals so that only small angle boundaries are present. Texture control is necessary to increase the average carrier mobility thus improving device performance and may also be useful in probing interface effects on charge carriers' transport. Furthermore, observations of growth on atomically flat silicon surfaces allow testing of theoretical predictions on the mode of growth of pentacene films.

Preferential azimuthal orientation has been observed in pentacene films deposited on mechanically rubbed polymer substrates and these films exhibited a

mobility anisotropy [18, 19]. However, the roughness and possible contaminants on the mechanically textured substrates result in lower quality films. An alternative that we describe here is to use the atomic steps on annealed, crystalline silicon substrates, to induce orientation texture in deposited polycrystalline pentacene films. To our knowledge, the only other report of azimuthal texture orientation obtained in this way for organic semiconductor thin films was published by Ossó et al. [20, 21] on hexadecafluoro-phthalocyanine deposited on annealed sapphire ($11\bar{2}0$) samples. Itaka et al. [22] using sapphire (0001) for pentacene deposition only observed improved crystallinity on annealed sapphire substrates (larger grains and better c* axis alignment). Previous attempts to use stepped Si (111) for texturing polycrystalline pentacene films did not work [23], probably because growth was only investigated over a limited temperature range.

4.2.2 Substrate preparation and pentacene deposition

The substrate used was Si (111) with a miscut angle of 0.1° – 0.5°. The thermodynamically stable vicinal surface consists of atomically flat terraces separated by bilayer atomic steps (0.31 nm in height). Such a smooth and clean surface can be produced by a high temperature anneal in ultra-high vacuum (UHV). Therefore, before performing the pentacene deposition, we modified the substrate morphology by high temperature annealing through direct current heating in UHV following the procedure detailed in the first chapter. The step flow, which takes place at the silicon surface during this high temperature anneal, shapes the surface morphology.

We used both lithographically patterned and unpatterned silicon surfaces. The patterned surfaces were comprised of craters of various shapes and sizes, etched in silicon using standard lithographic techniques. The main advantage of using patterned

samples is that a wide variety of surface morphologies, such as step free surfaces, regular arrays of parallel steps or step bunches separated by micron size flat terraces, can be obtained (as seen in the previous chapters). In this way, we can establish what would be the optimal step distribution for our substrates. The unpatterned samples are planar over their whole surface area and are thus better suited for ellipsometry or X-ray diffraction experiments; regular arrays of atomic height steps separated by atomically flat terraces are obtained, with the step separation determined mainly by the wafer miscut.

The annealed Si substrates, which acquire a 'native' silicon oxide top layer after removal from the UHV system, were given an UV/ozone treatment before pentacene deposition. The base pressure was below 10^{-6} Torr during the thermal vapor deposition of pentacene. A range of substrate temperatures, (90 – 130 °C), were investigated. The locations of the pentacene crystals relative to the steps as well as their shapes were investigated by atomic force microscopy (AFM), while the orientation of the pentacene crystals was investigated by grazing incidence X-ray diffraction (GIXD). The results presented below have been already published in Refs. [24].

4.2.3 AFM results

AFM analysis showed (Figs. 4.7(a), 4.8) that at deposition rates higher than 0.1 monolayer/ min (ML/min) the pentacene crystals deposited on stepped surface have a typical dendritic shape [25, 26]. At a similar temperature (~ 110 °C) but lower deposition rate (~ 0.05 ML/min) we obtained larger islands with a more rounded shape (Fig. 4.7(b)). At low deposition rates, there is probably enough time for the pentacene molecules attaching at the edges of growing crystals to migrate to higher coordination

sites, reducing the overall free energy of the crystal. While the AFM images do not show any obvious pentacene alignment, this does not mean that the pentacene crystals do not have a preferential texture alignment induced by the nucleation and growth at the steps. Even though the pentacene islands (one molecular layer height) spread out over many steps, they seem to nucleate with a higher probability on regions with higher step density.

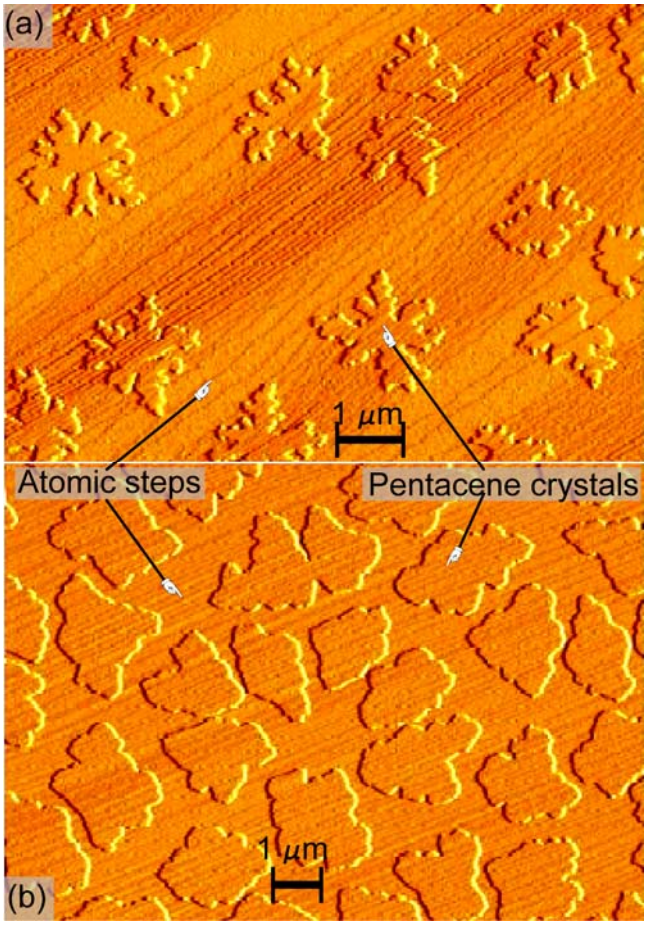

Figure 4.7. (a) At deposition rates of 0.1 ML (and higher) the pentacene islands acquire a dendritic shape during growth; (b) At lower deposition rate and higher temperature substrate, the pentacene islands are more compact.

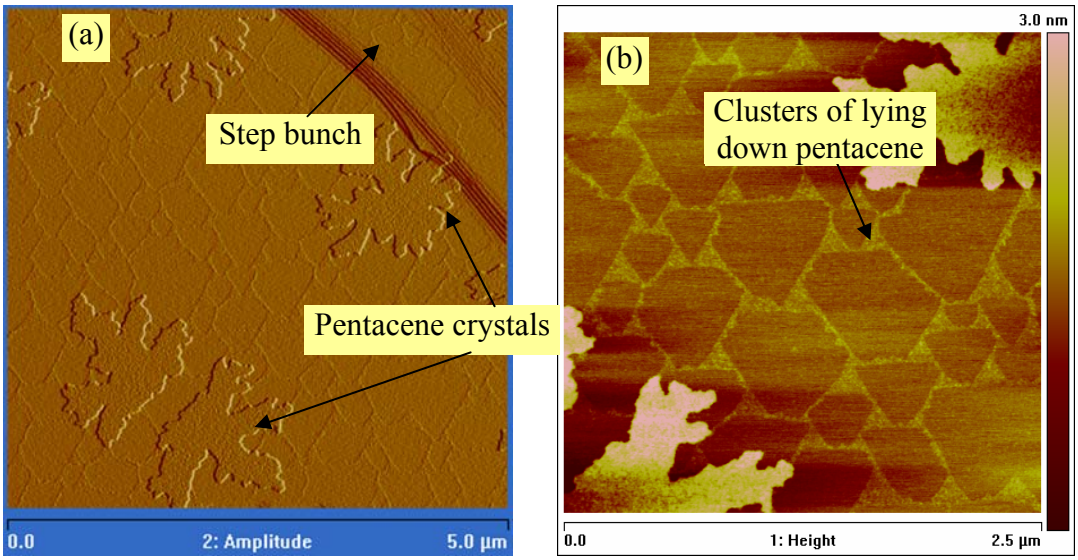

Figure 4.8. Pentacene deposited on a sample dipped in HF to remove the oxide layer. The islands have a dendritic shape. Pentacene molecules in lying down position decorate the boundaries of the (7x7) domains. Fig. 4.7(b) represent a detail from Fig. 4.7(a). The darker areas on the substrate are former (7x7) reconstructed regions and are not covered with pentacene.

A peculiarity of pentacene absorbing on flat silicon surfaces (with the native oxide layer removed by HF) can be seen in the Fig. 4.8. Apart from the large dendritic islands that have a height of ~1.5 nm, which correspond to the thin film phase (standing, slightly tilted molecules), one can see many narrow features with polygonal shape, about 0.3 nm in height. These regions correspond to the boundaries of (7×7) domains and are characterized by a high concentration of disordered adatoms [27]. In these regions, the high concentration of dangling bonds favor the clustering of flat lying pentacene. These features disappeared after the pentacene was removed by cleaning the sample with acetone in ultrasonic bath.

In regions where several atomic steps bunched into steep structures, we observed that pentacene crystals nucleate primarily along the steps (Fig. 4.9(a)). The deposition rate was again 0.05 ML/min and the substrate temperature 110 °C. The fact

that the terraces are several microns in width is what allows us to see that the pentacene nucleates preferentially at the steps. Such "optimal" substrate morphology occurs in certain areas of patterned silicon surfaces, where step flow caused by the high temperature annealing is influenced by the etched craters. In Fig. 4.9(b) we see the morphology of 3ML thick pentacene film deposited at 110 ºC on a silicon sample with a 0.1º miscut . The pentacene islands from the upper layer form facets that are often parallel or perpendicular to the substrate steps, even though the steps are usually only ~ 0.3 nm in height.

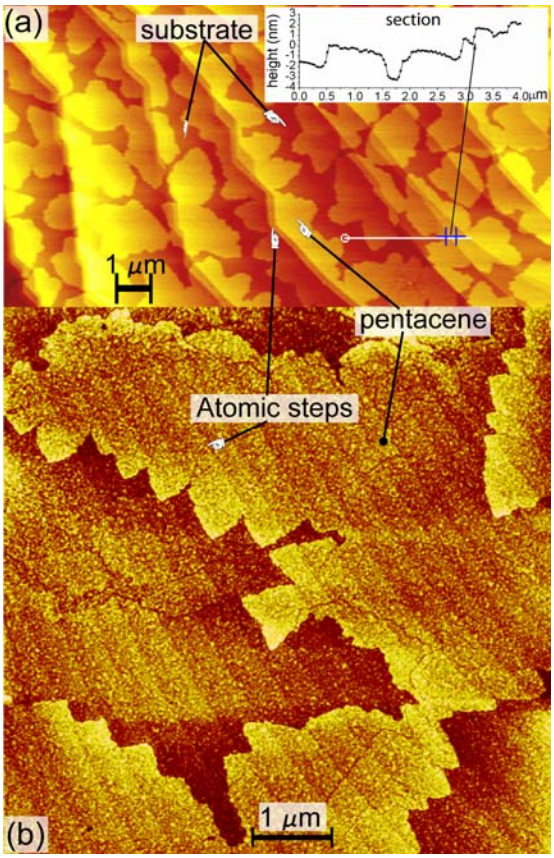

Figure 4.9. AFM images of sub-ML (a) and 3ML (b) of pentacene films deposited on stepped surface. (a) was obtained from a patterned sample where the step flow around the etched craters generated steep step bunches 1-2 nm in height, separated by wide atomically flat terraces. (b) was obtained from an unpatterned sample; the pentacene islands on the top layer form facets that align with the underlying substrate steps even though these steps are usually only one interplanar spacing in height (0.31 nm).

It is somewhat surprising that even when the step height is bigger than the length of the pentacene molecule (1.65 nm), the pentacene crystals seems to grow from the step edges on both the top and the bottom terraces (Fig. 4.9(a)). At the atomic level the step bunches are not however vertical but have a staircase structure; locally they are comprised of groups of several single, double, or triple height steps separated by nanometer scale terraces. Such a step bunch is probably a less effective nucleation site than a vertical wall but such a structure might allow pentacene islands to grow on both sides. From Fig. 4.9(a) it is nevertheless clear that nucleation has occurred preferentially along the step edges.

4.2.4. GIXD analysis

In order to explore the crystal orientation texture, in collaboration with Prof. Malliaras' group, we have performed GIXD measurements. The GIXD data presented in this section were obtained from the same sample shown in Fig. 4.9(b). The diffraction peaks obtained (Fig. 4.10) show a good crystallinity of the pentacene film.

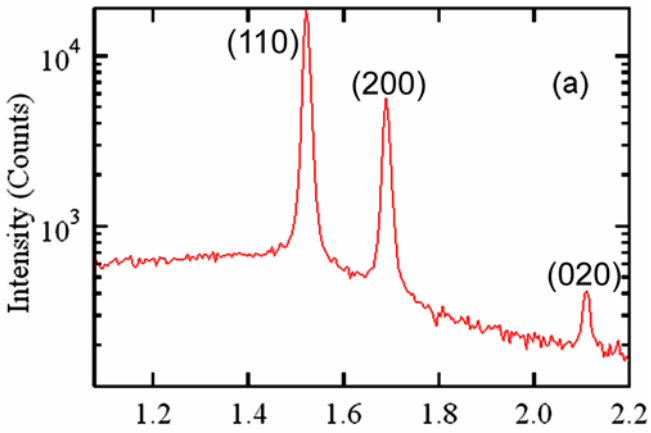

Figure 4.10. The intensity of the diffraction peaks versus scattering vector (in $Å^{-1}$) for a 3 ML thin film phase pentacene

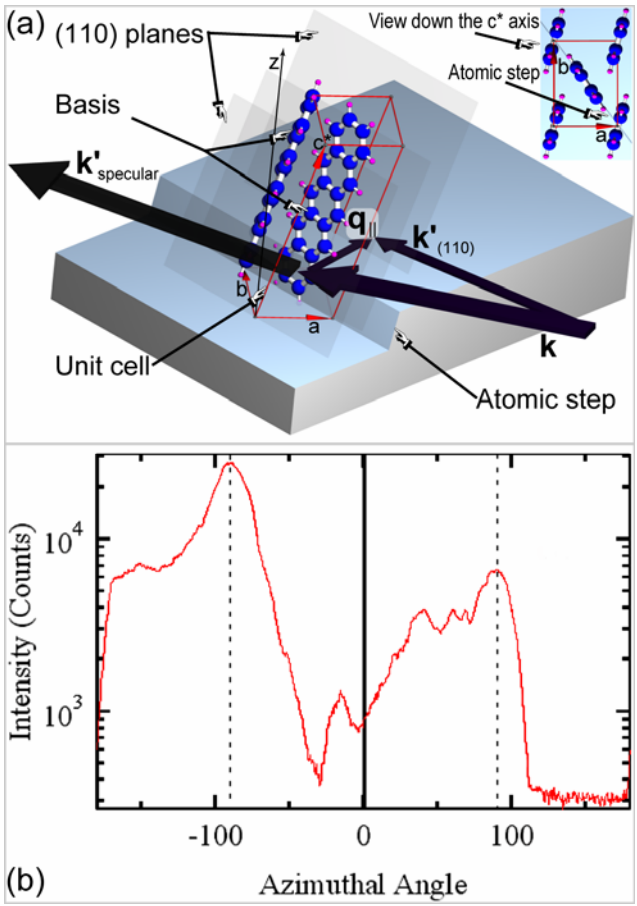

Figure 4.11. (a) GIXD geometry and the relative position of the pentacene molecules with respect to the atomic steps; (b) the in-plane anisotropy of the intensity of the (110) peak.

Fig. 4.11(a) indicates the geometry of the GIXD experiment. In this figure **k** is the incident wave vector, $\mathbf{k'}_{specular}$ is the specular diffracted wave vector, $\mathbf{k'}_{(110)}$ is the wave vector scattered by the (110) planes, and $\mathbf{q}_{\|}$ is the transfer vector corresponding to the beam diffracted by the (110) molecular planes. More details about the use of GIXD for investigating the crystallographic structure of the pentacene films can be found in Refs. [28, 29].

In order to look for preferred in-plane orientation, it is necessary to search for anisotropy in the intensity of a specific in-plane reflection (for example the (110)

peak) as the sample is rotated about the surface normal. The result of the (110) intensity as a function of azimuthal angle is shown in Fig. 4.11(b). If there was no preferred in-plane texture, the intensity of the (110) reflection would be approximately constant with sample rotation. As can be seen in our case though, there is a marked anisotropy with maxima approximately 180º apart as expected since there is no splitting of the {110} reflections due to $\gamma = 90^{\circ}$ in the thin film phase. However, the intensities of the two peaks are different, probably due to preferential direction of tilt of the (110) planes relative to the steps. Moreover, in the experiment the sample normal does not correspond exactly to the rotation axis with a miscut surface, the pentacene c* axis precesses about the surface normal; this complicates the quantitative analysis of the observed intensity anisotropy.

We believe that there are two main reasons why rather broad peaks are seen in Fig. 4.11(b). Firstly, while the step orientation is dictated mainly by the wafer miscut, there can be a fairly broad range of step orientation across the sample area. Secondly, some pentacene crystals grow from nuclei that are not associated with the atomic steps and these will be randomly oriented.

From the azimuthal position of the sample at which the maxima in Fig. 4.11(b) are obtained, we can deduce the average orientation of the (110) pentacene planes with respect to the general step direction. While a statistical average of the step distribution across the whole sample is very tedious to perform, a simple analysis shows that the (110) planes are mainly parallel (within $\pm 10^{\circ}$) to the atomic steps. This is consistent with the idea that the pentacene will align with the steps to maximize the van der Waals interaction; the (110) plane, being the most closely packed, might be expected to parallel the steps as shown in Fig. 4.11(a).

4.2.5. Discussions

While the UHV stage used in our work for the preparation of the Si substrate would be somewhat expensive, other simpler methods to obtain stepped surfaces on silicon, such as annealing in hydrogen, could be used (see for example Ogino et al. [30]). Sapphire is also an alternative substrate. Even though the distance between two nearest oxygen or aluminum (0001) layers is 0.216 nm, in certain ranges of the annealing temperature, steps are generally multiples of this 0.216 nm elemental spacing [31, 32].

It is interesting that Ossó et al. [20] reported 1.8 nm as the average step height on their sapphire $(11\bar{2}0)$ surface (the so called "A-plane"), similar to our "optimal" step-height substrate. Moreover in that experiment it was observed that step-induced alignment appears only in films deposited on a heated substrate (230 °C). We believe that the reason why Itaka et al. [22] did not observe any azimuthal alignment on the pentacene film grown on sapphire (0001) was that the substrate step height was only ~ 0.2 nm, the substrate was not heated, and the deposition rate (~1.5 ML/min) was much higher than in our case.

All these observations together suggest that to achieve well textured films the substrate should be heated, the deposition rate correspondingly limited and the average step height should ideally be comparable to the vertical dimension of the deposited molecules.

Further X-rays diffraction analysis combined with spectroscopic measurements are needed for a more quantitative characterization of the degree of pentacene crystals orientation. Mobility measurement would ultimately test if the pentacene thin films grown on stepped surfaces have enhanced mobility.

In summary, nucleation and growth of pentacene crystals along the atomic steps on Si(111) was observed using AFM in the special case when the height of the substrate steps is about the same as the height of the standing pentacene molecule. In the case of multilayer pentacene films, facets parallel to the steps are observed, confirming that even single atomic steps on the silicon substrate still function as a growth template for multilayer films. Carefully aligned GIXD experiments confirm the presence of preferred orientation and the results are consistent with the (110) pentacene planes being parallel to the atomic steps.

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APPENDIX A

FABRICATION OF MOS CAPACITORS

A.1 Patterning Si samples

1. Wafer preparation:

- RCA cleaning; wet oxidation at 1100 °C, anneal the wafer in N_2 also at 1100 °C (SiO_2 is used as etch mask for Si)

2. Mask preparation

- Design mask (pattern) with L-Edit (or Symbad) package
- Convert the GDS files into a PG file for GCA PG36000F Optical Pattern Generator
- Using this input data file, expose a chrome mask (with pre-spun photoresist) using the PG
- Develop the photoresist and etch the chrome using Hamatech-Steag Mask Processor (photoresist, mask etch and resist strip were done manually until about an year ago); inspect the mask

3. Wafer exposure

- Spray with acetone and IPA (isopropyl alcohol)
- Spin P-20 primer
- Spin Shipley 1813 photoresist at 3000 rpm for 30 sec.
- Pre-bake for 1 min at 90 °C on a vacuum hot plate
- Expose the wafers on the 5× g-line stepper (eventually run a focus and exposure matrix first)

- Post-bake the wafers for 60 sec at 115 °C on a vacuum hot plate
- Develop the exposed photoresist in 300 MIF for 90 sec.

4. Wafer etching

- Etch the SiO_2 using a CHF_3 (fluorine based) plasma (RIE)
- Dissolve the photo-resist in acetone or Shipley1165 resist remover (resist hot-strip bath)
- De-scum in oxygen plasma; rinse thoroughly
- Etch the silicon using a chlorine based plasma (RIE)
- Check the pattern (optical, profilometer, AFM, SEM)
- RCA cleaning

A.2 Second level lithography for building MOS capacitors

- MOS clean (RCA procedure) samples (remove the metal silicides that formed during high temperature annealing due to the contact with the sample holder and clamping springs); in order to reduce the surface roughening during the base bath (SC-1) cleaning, low base concentration has to be used
- Perform a furnace dry oxidation at 850 °C for 5 min in 20% O_2 / 80%N_2 (=> 3-4 nm oxide)
- Perform a H_2 anneal at 600 °C (to remove the interface traps)
- Check again the surface morphology (AFM)
- Use YES HMDS vapor prime oven to prepare the samples for exposure
- Spin photoresist

- Align the sample for this second level of lithography and expose them (second, negative mask)
- Use YES ammonia image reversal oven (ammonia binds with carboxylic acids that were generated in the exposed regions, making these regions insoluble).
- Flood expose on HTG contact aligner in order to expose previously unexposed regions (60 sec)
- Develop 1 min in MF321
- Descum in O_2 plasma and rinse with DI water (to assure good metal-oxide contact)
- Deposit Al using e-beam evaporator
- Lift –off using resist solvents (eventually in a ultra-sonic bath)
- Check the integrity of the capacitors (optical, SEM)
- Etch the SiO_2 from the back of the sample (fluorine based plasma etch)
- Deposit Al on the back of the samples (back contact)

APPENDIX B

MATLAB FUNCTIONS USED TO PROCESS DATA

B.1 Functions for generating temperature contour maps

```
function [C]=main_t(str,n1,n2)
%    MAIN--the main function;
%
%    []=main_t(str, n1, n2);
%    Receives a string for the file name and a range
[n1:n2]
%    Reads a corresponding range of data files and write
the
%    transformed data
%    onto HDD into the current directory

%    str=pad5_

B=zeros(40,60);
% creates a matrix of zeros containing 40 rows 60 columns
for i=n1:n2
    if i<10
        fname=[str,'_0',num2str(i),'.txt'];
% add zero before a one digit number
    else
        fname=[str,'_',num2str(i),'.txt'];
    end
    [A,l]=readt(fname); % read the i row
    B(i,1:l)=A; % copy into B the A row
    L(i)=l;
end
C=B(n1:n2,1:min(L));
%    save 'matrix_T.txt' C -Ascii -Tabs;
%    draw_Tcontour(D);
%    fn=[str,'_matrix','.txt'];
%    fid=fopen(fname,'wt');
%    if(fid<1)
%    error(['Unable to open ',fname]);
%    end
%    fprintf(fid, '%f\t', C);
%    fclose(fid);
```

```
function [C,l]=readt(fname)
%readdata--reads a data file; returns a raw vector
%
% A=readt(fname)
% Reads a file, fname, which contains three columns of
% data
% Retrieve the middle colomn with the temperature values
% Transform it into a row vector A
% uses fscanf function

% Returns an the row vector A


fid=fopen(fname,'rt');
if(fid<1)
    error(['Unable to open ',fname]);
end
for i=1:14;
    header=fgetl(fid);
% skip over the first 14 lines of file - header
end
[A,l]=fscanf(fid,'%i %c %f\n');
% load data into a column vector A
% each other third value is usefull
fclose(fid);
B=(reshape(A',3,length(A)/3)); % returns 3-by-(A/3)
matrix from A
C=B(3,:); % copies in C the third row
l=length(C);


function []=draw_Tcontour(A)
% draw_Tcontour--draw the contour plot of a matrix
%
% draw_Tcontour(Matrix)
% Plot the temperature contour using the temperature map
% stored in A
%
% Returns an the row vector A

figure; % creates a figure window
set (gcf, 'color','w');
% set(gca,'TickDir','out', 'xtick', [1:5:20]);
axes('position', [0.1 0.3 0.85, 0.5], 'FontSize',12);
% subplot(2,1,1);  % 2x1 plots, first half
cl = 1100:10:1210; % Define contour levels for all plots
```

```
% X = [0:0.5:12]; % X axix is from 0 to 12 mm
% Y = [0:0.5:6]; % Y axis is from 0 to 6 mm
% F = [1 1.5 1.7; 0.5 0.9 1.2; 1.3 1 0.2];
% specify a 3x3 convolution kernel for smoothing
% B = conv2(A,F,'same');
% smoothen data using F for convolution
[C,h] = contourf(A,cl);
% fills the area between contour lines
clabel(C,h, 'FontSize',14);
% labels the contour line
% caxis('auto');
colormap jet;
colorbar;
```

B.2 Functions for processing the acquired I-V data

```
function []=main(str,n1,n2)
% MAIN--the main function;
%
% []=main(str, n1, n2);
% Receives a string and an interval [n1:n2]
% Reads a corresponding range of data files and write the
% transformed data
% onto HDD into the current directory

%str=pad5_
for i=n1:n2
    fname=[str,num2str(i),'.data'];
    [x,y]=FN_transform(fname);
    s=find(fname=='.'); % change the extension
    name=fname(1:s);
    name=[name,'dat'];
    FN_write(name,x,y);
end


function [x,y]=FN_transform(fname)
%FN_TRANSFORM--reads a data file; returns two columns:
% V-voltage and I-current
%
% [x,y]=FN_transform(fname)
% Reads a file, fname, which contains two columns of data
% tab separated: I vs. V
% Returns a two column matrix
```

```
% the numbers from the first column are 1/V
% and the numbers from the second column are ln(I/V^2)
% Writes the numbers into a TAB delimited ASCII file
% uses fscanf function

fid=fopen(fname,'rt');
if(fid<1)
    error(['Unable to open ',fname]);
end
header=fgetl(fid);
[A,l]=fscanf(fid,'%f\t %f\n'); % load data into a column
vector A
fclose(fid);
B=(reshape(A,2,length(A)/2))'; % returns 2-by-A/2 matrix
from A
V=B(:,1);
I=B(:,2);
Idx=find(I>5e-12); % get rid of noise - keeping only
useful data
V=V(Idx);
I=I(Idx);
x=1./V;
y=log(I.*x.*x);


function fid=FN_write(fname,a,b)
%FN_WRITE--save the vectors a,b to a file fname; a=
%
% fid=FN_write(fname);
% Write the columns a,b vectors into a TAB separated
% ASCII file.
%
fid=fopen(fname,'wt');
if(fid<1)
    error(['Unable to open ',fname]);
end
A=[a';b'];
fprintf(fid,'%f\t %f\n',A);
fclose(fid);
```